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Design of NLMS adaptive filter architecture using backend VLSI technology

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ABSTRACT

The proposed NLMS techniques have been modeled using Verilog HDL; the models have been verified using test benches with a functional coverage of 95%. The results obtained have been compared with MATLAB results, which are considered to be a benchmark. The HDL (Hardware Description Language) code is synthesized using Synopsys Design Compiler targeting 130-nanometer TSMC (Taiwan Semiconductor Manufacturing Company) library and target technology. The synthesized netlist obtained for all the adaptive filtering techniques proposed in this research work is taken through physical design flow consisting of Floorplanning Placement and Routing steps. The results obtained at each step are simulated for the functionality. The final GDSII (Graphical Design Standard II) file is generated for the proposed techniques.. The floor planning, placement and routing of the netlist ensures that the overall size for the entire chip does not exceed by 2.15 Square millimeters. The results obtained for NLMS adaptive filtering techniques using pipelining, parallel processing, low power techniques and floating point architectures have proven that the complexities in the industrial applications can be met if the design is implemented on ASIC.

Introduction

One of the primary disadvantages of the LMS algorithm is having a fixed step size parameter for every iteration. This requires an understanding of the statistics of the input signal prior to commencing the adaptive filtering operation. In practice this is rarely achievable. Even if we assume the only signal to be input to the adaptive echo cancellation system is speech, there are still many factors such as signal input power and amplitude which will affect its performance. The normalized least mean square algorithm (NLMS) is an extension of the LMS algorithm which bypasses this issue by selecting a different step size value, μ(n), for each iteration of the algorithm. This step size is proportional to the inverse of the total expected energy of the instantaneous values of the coefficients of the input vector **x**(n). This sum of the expected energies of the input samples is also equivalent to the dot product of the input vector with itself, and the trace of input vectors auto-correlation matrix.

Design

The equivalent design architecture of NLMS algorithm is shown in Figure 1.1.

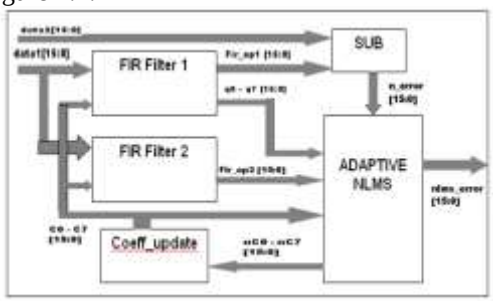

Figure 1.1 Design architecture of NLMS

As the NLMS is an extension of the standard LMS algorithm, the NLMS algorithms practical implementation is very similar to that of the LMS algorithm. Each iteration of the NLMS algorithm requires the following steps

1. The output of the adaptive filter is calculated.

$$y(n) = \sum_{i=0}^{N-1} w(n)x(n-i) = \mathbf{w}^T(n)\mathbf{x}(n) \quad (1.1)$$

2. An error signal is calculated as the difference between the desired signal and the filter output.

$$e(n) = d(n) - y(n) \quad (1.2)$$

3. The step size value for the input vector is calculated.

$$\mu(n) = \frac{1}{\mathbf{x}^T(n)\mathbf{x}(n)} \quad (1.3)$$

4. The filter tap weights are updated in preparation for the next iteration.

$$\mathbf{w}(n+1) = \mathbf{w}(n) + \mu(n)e(n)\mathbf{x}(n) \quad (1.4)$$

Each iteration of the NLMS algorithm requires 3N+1 multiplications, this is only N more than the standard LMS algorithm. The NLMS algorithm shows far greater stability with unknown signals. This combined with good convergence speed and relative computational simplicity makes the NLMS algorithm ideal for the real time adaptive applications.

Simulation and Backend Results

The simulation results obtained from the Modelsim is shown in Figure 1.2

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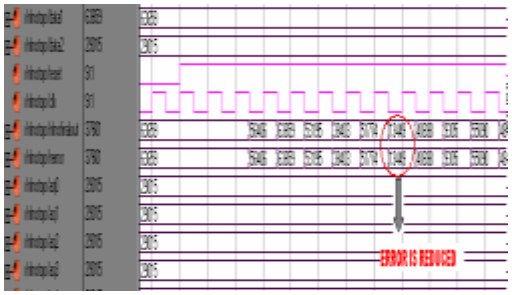

Figure 1.2 Simulation report of NLMS architecture.

With functional verification the design is ready for physical implementation, the first step in physical implementation is to use the HDL model developed and convert it to an RTL code that can be synthesized. Hence the RTL model is synthesized using industry standard EDA tool called as Design Compiler from Synopsys. DC is a sign of tool for synthesis, in this process the RTL model is converted to gate level netlist. The gate level netlist should be able to meet area, timing and power requirements.

Optimization constraints include operating frequency (clock period), input and output delays at the IOs. For the present work TSMC 130 nanometer target technology is adopted for better performances. The constraints mentioned for the design are maximum operating frequency 93.9 MHz, total number of gates not to exceed 109,324 cells, and power not to exceed more than 75 mW. The Figure 1.3 shows the schematic, which was generated after synthesizing the RTL code.

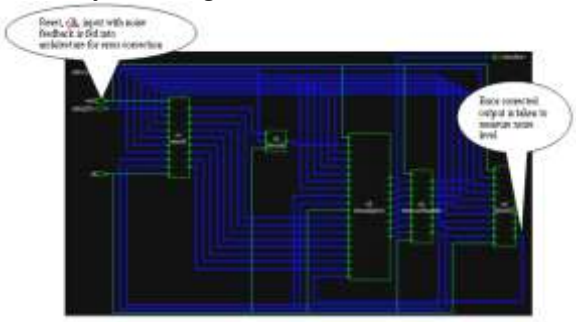

Figure 1.3 Synthesized schematic of NLMS architecture

The constraints mentioned select the required gates from TSMC 130 nanometer library. The design requires 4 inputs and produces 1 error corrected output.

REPORT	NLMS
slack	0.01
Maximum critical paths	128
Number of ports	50
Number of nets	562
Combinational area	72990
Sequential area	8354
Total area	111090
Total Dynamic Power	75mw
Total Dynamic Power	180.3 uw

Table 1.3 Report of NLMS architecture

NLMS architecture requires less cell area, has 562 total numbers of nets to be routed and consumes 76mwatts of power at 1pf capacitance load.

However, these effects are being suitable reduced to a large extent by adopting optimized ASIC design methodology extent with proper floorplanning , placement and routing being done semi automatically the total die size for NLMS architecture with the die size of 1.755*1.755 , the final chip is shown in Figure 1.4.

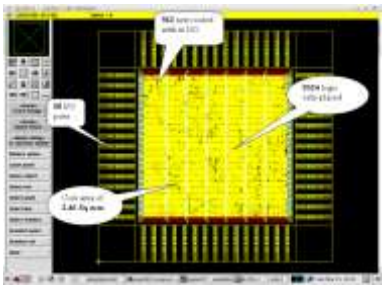

Figure 3.26 Top view of the entire NLMS die with logic cells and I/O cells

Conclusion

Adaptive noise cancellation techniques such as LMS and RLS have been extensively used for noise cancellation techniques with good performances. These techniques have been extended for use in industrial applications, wherein there is a need for accuracy, speed, reliability and cost. Algorithm such as NLMS has been realized on ASIC. The proposed architectures has been modeled and verified for its functionality successfully. The models have taken through the entire ASIC flow. Suitable results are obtained at various stages of the ASIC flow using Synopsys.

The signal sampled at 1K samples per second has a data rate of 16 Kbits per second when fed through the proposed hardware which produces an output at 16 Kbits per second with latency of 8 clocks and throughput of 1 clock cycle. The proposed techniques have been modeled using Verilog HDL and compared with MATLAB results, which are then synthesized using Synopsys Design Compiler targeting 130-nanometer TSMC library and target technology. The synthesized netlist obtained for the NLMS adaptive filtering technique proposed in this research work is taken through physical design flow consisting of Floorplanning, Placement and Routing steps. The results obtained for NLMS architecture outperform at the speed of 94MHz. The overall size of the entire chip is 2.46 sq mm with a gate count of 109324.Constraints such as area, power and frequency have been used to optimize the design. A tradeoff between all the three have been identified and documented

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