Available online at www.elixirpublishers.com (Elixir International Journal)

Power Electronics Engineering

Elixir Power Elec. Engg. 35 (2011) 2833-2835

ISSN: 2229-712X

Modelling and characterization of DCO using Pass Transistors

E.Kanniga[1] and M.Sundararajan[2]
[1]Department of ECE, Bharath University, Chennai-73
[2]Gojan School of Business & Technology, Chennai-52.

ARTICLE INFO

Article history:
Received: 6 April 2011;
Received in revised form:
19 May 2011;
Accepted: 26 May 2011;

Keywords
Digital controlled oscillator,
Steady state transient response,
Simulation LTSPICE,
Varactors.

ABSTRACT
In the field of simulation work, it could proceed to an extent that, simulate with arbitrary values of the passive component and the voltage sources. The simulation results recorded various strategic points in the circuit indicate and validate the fact that the circuit is working in the expected lines with regard to the energy transfer in the expected lines with regard to the energy transfer in the tank circuit and sustenance in DC transient Analysis. Also in this proposed experimental work, it is observed that for an arbitrary load, the voltage obtained is agreeing with the theoretically computed DC-Voltage levels. The scope of the work can be extended to the actual calculation of the passives, the initial voltages across the capacitors and inductors. In addition to the exciting DC levels of the sources employed. The small signal analysis can also be done with due regard to the desired behavioural properties of switching devices used.

ntroduction

In the digital world there is an increased requirement for Digitally Controlled Oscillator (DCO).

The Traditional DCO core with Inductor Capacitor (LC) tank biasing network still makes it complicated with Analog Analysis. Therefore to make it fully digital one can take up a design with pass transistor.

Varactors

Varactors are a principal component of LC Voltage Controlled Oscillator (VCOs) used for frequency fine tuning. Digitally controlled switched varactors or switched capacitors could also be used for coarse tuning in some designs. [2]

NMOS (N type metal oxide semiconductor) transistor, with gate as the first terminal and drain, source, and bulk connected together to form the second terminal. MOS varactors operate in four main regions, based on the biasing point (voltage across the varactor terminals) accumulation, depletion, weak inversion, and strong inversion.

Accumulation and strong inversion are two regions where most varactors are designed to operate in. Furthermore, a study on accumulation-mode and inversion-mode varactors reveals that LC oscillators based on accumulation-mode varactors demonstrate lower power consumption and lower phase noise at large offset frequencies from the carrier, compared to those based on strong inversion.

In most of the applications, designers would like to ensure that the capacitance of the varactor is a monotonic function of the biasing voltage. For instance, in an LC VCO, it would be desirable to have the varactor operating predominantly in accumulation mode. However, using a regular NMOS does not warrant this, as the operation region is voltage dependant. It is also worth noting that the C-V (Current Voltage) curve of a regular nMOS is frequency dependant. It may seem similar to an NMOS transistor; however, the *n*+ regions have been buried in *n*-well, instead of *p*-well. This configuration guarantees that the device does not enter the inversion-mode at all; hence the name accumulation-mode

Fig1 shows that NMOS transistors configured as a Varactor

Fig.1 Symbolic representation Varactor

In most applications, designers would like to ensure that the capacitance of the varactor is a monotonic function of the biasing voltage.

Fig2. Show that the C-V characteristics of an MOS varactor can be predicted using 2D/3D numerical simulators. Unfortunately these simulation tasks require precise knowledge of the underlying doping profiles which usually are not readily available. An alternative is to perform capacitance measurements. However sub Pico Farad capacitance is difficult and requires a fairly expensive S- parameter RF measurement setup. It is therefore very useful to predict the tuning characteristics of LC Oscillators. Using standard foundry supplied models for MOSFETS.

Recently, a lot of effort has been expended on modelling the C-V characteristics of MOS varactors.

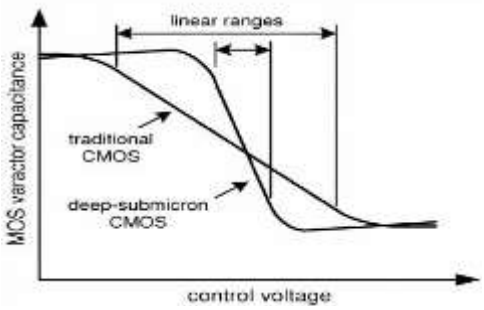

Fig.2 C-V Characteristics of MOS varactors

Pass Transistor

Fig 2 shows that schematic representation of a pass transistor.

Tele:
E-mail addresses: Kannigatruth@yahoo.com

A Pass transistor is a MOSFET in which an input is applied not only to the gate, but also to the drain. The principle is taken up from the multiplier circuitry. In the multiplier circuit pass transistors are used to reduce the layout complexity. This is done by pass transistors connected to pass a first and second input function to an output node in response to a selected output function on the output node.

The PASS transistor comprises a transistor capable of passing an input function in response to a CONTROL signal applied to the transistor, thereby to generate an output function related to the input function.

The challenge is to replace the capacitor bank (or) the variable capacitor by Transistor. A pass Transistor is a MOSFET in which an input is applied not only to the gate, but also to the drain.

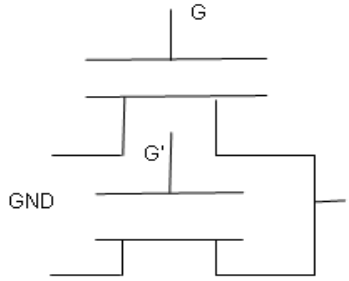

Fig.3 schematic representation of a Pass Transistor

DCO Design and tuning Characteristics

Conventional VCO's use the Analog voltage control for frequency tuning. Analog frequency tuning not compatible with deep submicron CMOS processes.

- o Varactors highly nonlinear.
- o Voltage headroom squeezed.
- o Analog voltage resolution unreliable
- o Analog interface difficult for integration.

DCOs use digital approach for frequency tuning.

- o Easier implementation in advance CMOS processes.
- o Allowing fully digital implementation of the PLL loop control circuitry.

The proposed architecture may be successfully implemented for RF application. Differential LC tank Oscillators remain as the standard choice for the oscillator core. Digital control realized by individually switching an array of capacitance devices in the LC tank. Cross coupled MOS gain stage for negative resistance. Capacitance implementation using MOS Varactors (switched capacitors) array may be used to augment the tuning range high –Z tank to improve effective loaded tank Q. Biasing current digitally tuned for performance optimization.

Digitally controlled switched varactors or switched capacitors used for coarse tuning in some designs.

In DCO design and tuning characteristics, the closed loop system oscillator has to fulfil the following Bharkhausan conditions at all times for continuous oscillation.

$$|H(j\omega)| > 1$$

$$< H(j\omega) = 360 \text{ (or)}$$

$$< H(j\omega) = 0 \text{ ---------} \rightarrow 1$$

Where H(jω) is frequency response

The Modelling of the tuning characteristics is a straight forward task, as the oscillation frequency (f_{osc}) is given by the following well known formula,

$$f_{osc} = \frac{1}{2}\Pi\sqrt{LC(v)} \text{ --------} \rightarrow 2$$

Where L is the inductance C (v) is the equivalent capacitance for a given biasing point. The equivalent capacitance can be extracted using

$$c(v) = \frac{1}{4}\pi^2 f_{osc}^2 L \text{ ------} \rightarrow 3$$

Having determined c (v) values in eqn (3), an extracted piece wise linear model of the voltage dependent capacitance is reconstructed and fed back to LTSPICE for simulation.

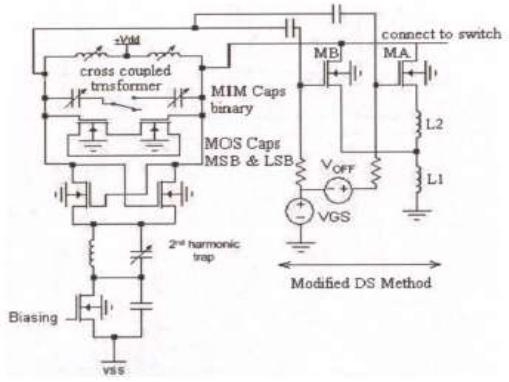

Fig.4 Detailed Circuit diagram of DCO

In DS method, the magnitude and phase of second order nonlinearity contribution to M3 components is tuned to cancel the third-order nonlinearity contribution to M3 components, thus resulting in an output current with a minimum M3 component. As shown in fig4, the transistor MA is biased in the strong inversion region, while MB is biased in weak inversion. The two source degeneration inductors L1 and L2 connected to the sources of the two transistors are used to tune the magnitude and phase of the 1M3 components. [Ref.1]

The challenge is to replace the capacitor bank or the variable capacitor

Fig.5 Block Diagram of proposed DCO

Basic theory

The MOS M1 acts as control switch to gain control over the switching of the circuit such that the switching is done by controlling the gate voltage given to it turns on the MOS which grounds the entire circuit voltage from the tank circuit to prepare for full cycle of operation.

The tank circuit F2 enables the selective grounding and control of the oscillations of a particular frequency to pass through the M1 transistor so that the selective tuning is made possible.

The transistors M2 and M3 are the cross – coupled giving rise to a perfect matching of the isolation provided by M4 and M5. MOS transistors offer high input impedance that makes its usage as a much preferred input stage of many devices and circuits to avoid direct grounding of the actual resonance circuits.

The resonance circuits provide the energy sustenance to provide oscillations of the desired frequency, which is passed to the load through a ground noise filtering circuit so as to eliminate ground noise, which is much prevalent in circuit when implemented in the printed circuit boards... The ground traces offer a certain amount of resistance to the signals which need to be protected against the noise to maintain signal quality and strength.

Experimental Set and Result Analysis

Arbitrary selection of components and their values need to be done based on the small signal analysis of the circuit and the time domain transient analysis results.

Basically, the two tank circuits that are used in the circuit involve small values of inductors and capacitors which can be tuned or changed depending upon the range of oscillations required. The oscillation frequency can be found from the afore mentioned analysis using small signal model of the circuit.

The ac component part of the equation(1), when let to zero, yields the value of ω, which is a function of the passive components such as L and C (including R, which is a damping component in the oscillations generated)

This ω, is taken as reference radians that would give the value of the exact frequency of oscillations to which the circuit need to be retuned and redesigned for every simulation run done.

The permutation and combination possibility of the number of instances of change in the LC is given as 24. However, since two of the tank circuits are LC for producing sustained oscillations, the values have to be chosen based on the small signal analysis. Thus approximately 10 combinations of L and C can be tried for various settings.

The capacitors C4 and C5 are to be replaced using the values as given by the equation of frequency of oscillations. These capacitors would be replaced by the varactor diodes of the same value available in the market.

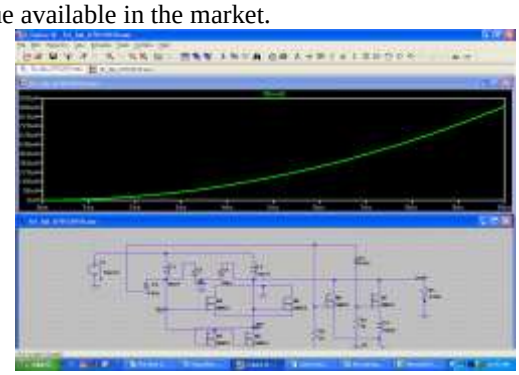

Fig. 6 The probe for one setting of the L and C and the excitation voltage

X axis(Time)	Y Axis(excitation Voltage)
0.91µs	0.083mv
1.33µs	0.041mv
3.05µs	0.0083 mv
4.00µs	0.000 mv

Table1. Excitation voltage Vs Time

Shown above in fig (6) is the voltage observed through the probe for one setting of the L and C and the excitation voltage. Simulation can be done for various values of L and C by change in the settings and the diode. The different values are tabulated in table1

Variation in Gating Signal means variation in the output. As we have seen, passing an input function in response to a CONTROL signal applied to the transistor, thereby to generate an output function related to the input function. In this project the focus is to utilize this quality of the pass transistor in the design of my DCO by having a Gating signal which will help to provide the required output.

The resonance circuits provide the energy sustenance to provide oscillations of the desired frequency, which is passed to load through a ground noise filtering circuit so as to eliminate ground noise, which is prevalent in circuit when implemented in the printed circuit boards. The ground traces offer a certain amount of resistance to the signals which need to be protected against the noise to maintain signal quality and strength.

Advantages

->power supply requirement is reduced

->power dissipation is reduced

->switching time is reduced

->interference between the components is reduced

LTSPICE

Linear Technology Corporation has launched the LTSPICE simulation. This simulation tool is efficiently used for the analysis of range, sampling, frequency, switched mode power supply, high speed CMOS, data compression, timing analysis, instant design files, etc.... than PSPICE

Conclusion

Brief description of the digital – controlled oscillator model is given. The model described in this article is primarily intended to be used for study of the digital controlled oscillator step response in LTSPICE environment. The model is based on idea that step response of a real digital – controlled oscillator can be well modelled as a steady state response.

References

1. Azar Hosseini, Hossein Gharaee, " Optimum Quad Band DCO in DS Method for WCDMA Transmitter in 90nm CMOS", Proc. 2008 Shariaty University, Tarbiat Modares University, *lohor* Bahru, Malaysia, page 44-47, ICSE 2008.

2. Pedram Sameni, Chris Siu, ShahriarMirabbasi, Hormoz Djahanshahi, Marwa Hamour, Krzysztof Iniewski, and Jatinder Chana, "Modeling and Characterization of VCOs with MOS Varactors for RF Transceivers", EURASIP Journal on Wireless Communications and Networking, Article ID 93712, Hindawi Publishing Corporation, Canada, Pages 1–12, Volume 2006.