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A survey on topologies of multilevel inverters

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ABSTRACT

Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power system. They give low harmonics, smaller distortion even at low switching frequencies and has low commutation loss but they suffers from complexity problem requiring large number of power devices and complex control algorithm. This paper presents some important topologies like diode-clamped(neutral -point clamped), capacitor-clamped (flying capacitor), and cascaded multicell inverter with separate dc sources and comparison between these topologies is done on the basis of total loss and estimated cost of each topology .Other emerging topology and modulation schemes are also discussed along with their advantages.

Introduction

In Recent Years, industry has begun to demand high power equipment, which requires power in megawatts. Controlled ac drives are usually connected to the medium-voltage network. So, it is hard to connect a single power semiconductor switch directly to medium voltage grids For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. Some of the important feature of multilevel inverters are they can generate output voltages with extremely low distortion and lower dv/dt, draw input current with very low distortion, generate smaller common mode (CM) voltage and can operate with a lower switching frequency.

Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. Fig. 1 shows a schematic diagram of a Multilevel Inverter with different numbers of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions. A Seven level inverter generates an output voltage with seven values generated by different output voltage with Seven values generated by different combination of the switches [see Fig.1 (a)], while the n-level inverter generates n-values [see Fig.1 (b)], and so on. By increasing the number of levels in the inverter, the output voltages have more steps for generating a staircase waveform which reduces harmonic distortion.

However, a high number of levels increases the control complexity and introduces voltage imbalance problems. Three basic topologies proposed for Multilevel Inverter are Diode-clamped (neural clamped), capacitor clamped (flying capacitors) and cascaded multicell with separate dc sources [1]. In addition, several control strategies are also developed or adopted for multilevel inverters including the following: Reversing voltage [2], Space vector control [3], Novel based Cascaded Multilevel inverter [4] along with some modulation schemes [5].

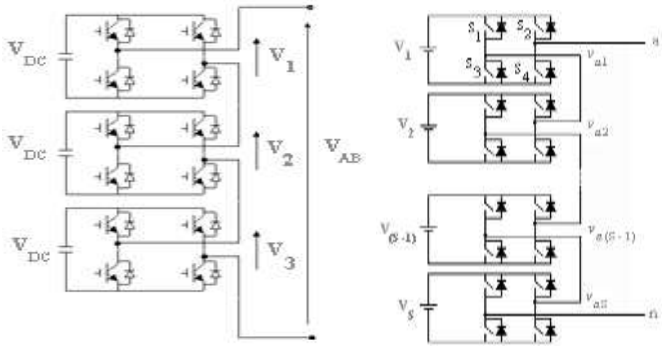

Fig. 1 Multilevel Inverter (a) Seven levels, (b) n levels

This paper is divided into three sections. In the first section basic topologies for Multi level inverter is discussed and comparison between them is done on the basis of total loss and estimated cost. Then emerging topologies were discussed along with advantages of each. Finally modulation schemes for Multi level inverter are described.

Inverter Topologies

Basically there are three main circuit topologies for Multi level inverter .Diode clamped inverter, which uses concept of using diodes to limit power devices voltage stress. It consists of series connected capacitors that divide DC bus voltage into a set of capacitor voltages. Second topology is Capacitor clamped inverter in which capacitor is used instead of diodes for limiting voltage stress. Size of voltage increment between two capacitors defines size of voltage steps in output voltage waveform. However additional circuit is required for initial charging of capacitors. Third topology is the Cascaded cell topology in which several single-phase H-bridge inverters are connected. It eliminates the excessively large number of clamping diodes required by the DCMLIs and capacitors required by the CCMLIs. Also it provides flexibility in extending to higher number of levels without undue increase in circuit complexity.

Diode Clamped Multi-Level (DCMLI) Inverter

In this topology, some DC-link voltage potentials are connected through the clamping diodes to the output. In each phase leg, the forward voltage across each main power device is

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clamped by the connection of diodes between the main power devices and the nodes.When DCMLI has more than 4 levels, several clamping diodes must block more than two times the voltage of main device's collector-emitter voltage (Vce). That is why these diodes are connected in series. Moreover, this topology has still severe problems with DC-link voltage control. In order to keep each DC-link capacitor's voltage equal, an IGBT with anti- paralleled diode is used instead of the clamping diode. DCMLI has the advantage of low switching frequency and all the three phases have same common DC link capacitors. Also reactive and negative-phase sequence current can be controlled in DCMLI. However requirement of large number of diode for clamping makes the physical layouts difficult e.g. increase stray inductance.

Flying Capacitor Multi-Level Inverter (FCMLI)

At first, FCMLI was proposed as a chopper. In this topology, the clamping capacitors are used to step down the DC-link voltage to the adequate voltage. When an adequate modulation is used, these clamping capacitors are automatically balanced. The disadvantage is that the clamping capacitors become large, when switching frequency is low, because the output current flows through a clamping capacitor as long as the switching state does not change. Also it requires excessive number of capacitors for clamping.

Cascade Cell Multi-Level Inverter (CCMLI)

CCMLI was proposed at first in [4]. In this topology, no clamping component is necessary. This is a big advantage; however, each inverter needs separate DC-link capacitors. That's why this inverter can control only reactive current, when it is operated individually (i.e. it does not require any active power source). To compensate the negative-phase sequence current, the control method used in thyristor-controlled shunt compensators can be used. The current rating of the inverter must be more than double of the negative phase sequence current to be compensated. These three types of inverters were designed for a 6.6 kV -12MVA STATCOM and the operational loss and cost were compared

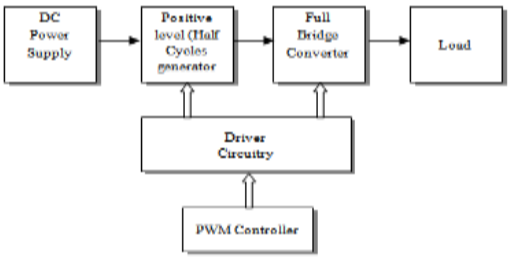
Operational loss: The total loss of the DCMLI is lowest; however, maximum junction temperature among all IGBTs is the highest. Therefore, it is difficult to optimize the heat sinks. The CCMLI has the highest total loss, even though the loss of each IGBT is minimum, because there are twice as many IGBTs as in the other topologies. Finally each IGBT in the FCMLI has homogenous losses and the total loss is smaller than CCMLI´s. Thus, it is clear that FCMLI is the most attractive topology in the comparison of operational losses. Comparison is shown in Table I.

Cost evaluation: DCMLI is the most expensive and the cost of the CCMLI and the FCMLI is almost equal. In the DCMLI, the clamping diode´s cost is about 10% of total cost. Moreover the DCMLI makes the bus bars complex and expensive so it needs more space, i.e. more cabinets. The CCMLI should be much cheaper than the others as it does not need any clamping devices and the bus bars can be compactly constructed. However this delta connection CCMLI needs twice as many IGBTs as other topologies so it becomes more expensive for the specified application. FCMLIs need clamping capacitors; however they are cheaper than diodes. In addition, the bus bar is not so complicated. Even though the FCMLI needs extra capacitor bank in order to store the DC-link capacitor and several clamping capacitor so it is more attractive than DCMLI. Comparison is shown in Table II.

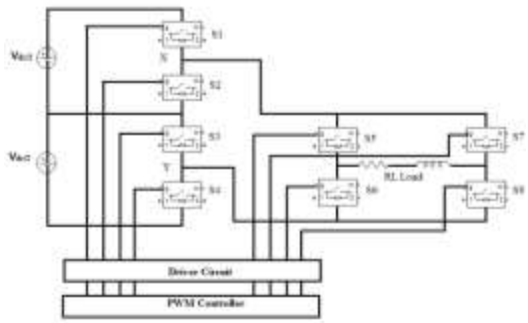
Emerging topology and strategies

Reversing Voltage Topology

The block schematic of Reversing Voltage topology for multi-level inverter is depicted in fig. 2. The principle idea of this topology as a multi-level inverter is that the left side stage in fig.2 (a) generates the required positive levels and the right side circuit of fig. 2(a) reverses the voltage direction when the voltage polarity requires to be changed for negative polarity.(Negative half cycle of the fundamental output voltage).



2(a)



2(b)

Fig 2 Reversing voltage topology (a) Block diagram of inverter using reversing voltage topology (b) Schematic of single phase five level inverter for RL load

Operation of the presented topology can be easily explained with the help of fig. 2 and table III. When S1 and S4 are turned "on" the output voltage Vxy is Vdc as shown in fig 2(b). The output voltage Vxy will be Vdc/2 when switches S2 and S4 are turned "on ". By proper switching combinations of S1, S2, S3 and S4, the positive half cycles can be generated. Switch S5 and S6 are complementary, similarly S7 and S8 also for a complementary pair. When S5 and S8 are switched "on "together (for duration 10 ms or half cycle duration of fundamental output voltage), positive half cycle can be generated and when S6 and S7 are switched "on" together (for duration 10 ms) negative half cycle can be generated across load The voltage blocking capacity of each switch is Vdc/2.This topology requires half of the carriers as for PWM.

High Performance Switching Strategy for Vector Control Method:

This switching strategy for multilevel cascade inverters is based on the space-vector theory. The proposed strategy generates a voltage vector across the load with minimum error with respect to sinusoidal reference. In addition, it generates very low harmonic distortion operating with reduced switching frequency without the use of the traditional sinusoidal pulse width modulation techniques or more sophisticated vector modulation methods. One of the most successful topologies used today in MV-ASDs is the cascade multilevel circuit (CML), which uses several low-voltage cells, each one containing an H-bridge inverter [6], [7]. Recently, the space-vector modulation

technique has also been successfully applied in CML inverter shown in fig 3(a). With this method, the power switches operate with relative high frequency. The number of steps in the Phase to Neutral N and Phase to phase voltages are shown in Fig 3(b). For example, with one cell per phase Van has only three levels $+V_{cc}$, 0, and $-V_{cc}$. In this connection phase to phase voltage V_{ab} has five different levels $+2V_{cc}$, $+V_{cc}$, 0, $-V_{cc}$,$-2V_{cc}$. The connection of a cell in each phase adds two more levels to the phase voltage Van and four more level in phase to phase voltage V_{ab}. The number of level in phase-neutral voltage V_{an} is given by

$$k = 2.p + 1$$

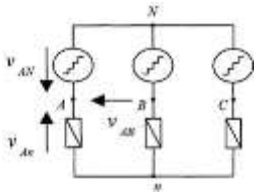
where p is the number of cells per phase. In addition, the Number of steps in the phase–phase voltage is given by

$$q = 2k - 1$$

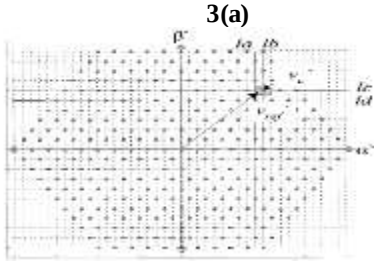
Each phase can generate 11 different voltages, which correspond to the 11 levels. The three-phase inverter can generate a total of 11.11.11 space vectors. The representation of the voltage vectors in the complex plane considers that

$$v(t) = v_\alpha + j.v_\beta$$

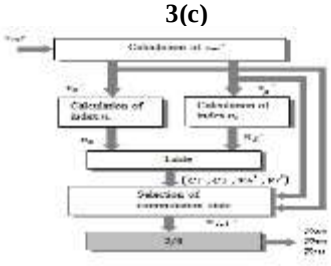
The main idea in the proposed control strategy is to deliver to the load a voltage vector that minimizes the error with respect to the reference voltage vector. For example, vector generated by the CML inverter has the smallest error with respect to the reference vector and this vector will be generated by control strategy. The high density of vectors generated by the 11-level inverter will generate small errors in relation to the reference vector. In order to make the appropriate vector selection, the real axis in Fig. 3(c) is divided into 40 different sections and the imaginary axis is divided into 20 sections. The boundaries la, lb, lc and ld shown in Figure 3(c) clearly identify the shaded rectangle, where the reference vector and the nearest inverter vectors are located. The real and imaginary part of are used to address a table containing vectors v´h and v'l shown in fig 3(d). The indexes for this table are then calculated .The next step is to compare the reference vector with the unique trace in the shaded area, to select the nearest inverter vector.



3(a)



3(c)



3(d)

Fig 3 Vector control method (a) Simplified circuit of CML inverter (b) Number of steps in CML inverter voltages (c) Normalized voltage vector generated by CML inverter (d) Block diagram of the control method

The trace is identified by the following equation:

$$y_1 = c_1.\alpha' + c_2$$

The coefficients c_1 and c_2 are contained in the same table. Finally, the decision between v'_h and v'_l is performed utilizing the following relation:

$$v'_\beta > c_1.v'_\alpha + c_2 \quad \text{then } v'_s = v'_h \quad \text{else } v'_s = v'_l$$

Novel Multilevel Inverter:

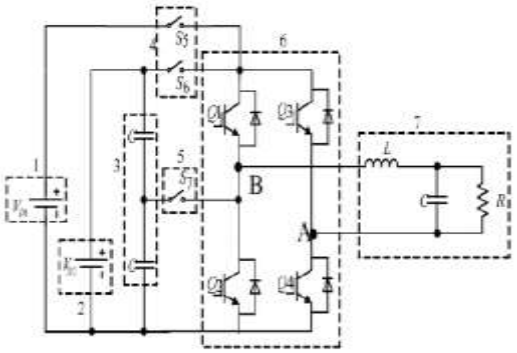
This is an alternative topology of hybrid cascaded multilevel inverter to reduce the number of required power switches compared to the traditional cascaded multilevel inverter and the modified PWM technique is developed to reduce switching losses. Multilevel inverter with two independent DC voltages sources that have similar configuration are utilized for the purpose as shown in fig 4(a).

The proposed multilevel inverter can synthesize a 7-level output. This configuration will be adequate for low- medium power UPS system.

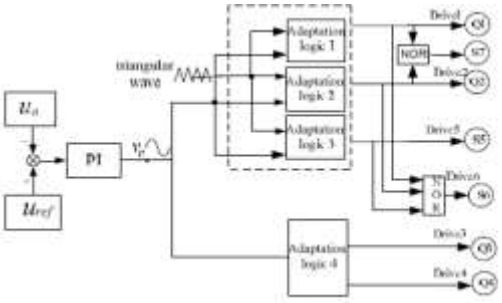
First of all, logical partitioning of the reference signals is determined according to number of output voltage levels and amplitude modulation as shown in fig 4(b).

When the reference signal is greater than zero and is in the C region, Q3 is turned on, Q4 is turned off. On the contrary, when the reference signal is less than zero and is in the D region, Q4 is on, Q3 is turned off. After the reference signal is entering the C range from 0 as shown in fig 4(c), we compare the reference signal with the carrier1 to get the drive signals of S6 and S7, the drive signal of Q1 is complementary with (S6 + S7), then the output is two level for 0 and C1; When the reference signal is in the B area, compare it with the carrier 2, to get the driver signals of S5, S7. S6 and S5 are complementary each other.

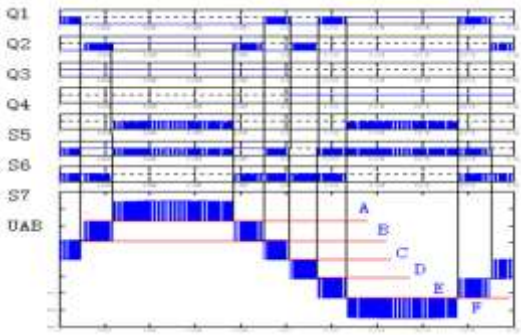
At this area, the bridge output level is C2 or C1 when the reference signal is into the area A, compare the reference signal with the carrier 3, to get the driver signals of S5 and Q2. S6 is complementary with S5, at this area, the bridge output level is C3 and C2; where the C1, C2 and C3 is triangular carrier with the same amplitude and phase exactly, but different position. When the reference signal enters into the negative half cycle in the D area, we compare the absolute value of it with the carrier 1 to get the drive signal of Q2. Drive signal of S7 is complementary with of Q2, at this area, the bridge output level is -0 and -C1. In the area E and F, the corresponding switch signals can be obtained by the same method.



4(a)



4(b)



4(c)

Fig 4. Novel based multilevel inverter (a) Switching circuit (b) Control block diagram (c) Inverter switching waveform

Modulation Schemes:

Modulation schemes for Multilevel inverter comes under two category Fundamental switching frequency and high switching frequency PWM. Classification of these schemes is shown in fig 5(a).

Step wave modulation:

It is a simple method by using the staircase waveform to approach the sine wave, which is a comparatively visual way as shown in fig.5 (b). In this method, the duration time of each level can be selected in order to eliminate some low-order harmonics, more the voltage level is, the better spectral characteristics can be gained. On the other hand, it is difficult to achieve the dynamic adjustment on the output waveform, which means it is not able to build an effective closed-loop control.

Selective Harmonic Elimination Modulation:

It has also been called as the "Switch-point Preset PWM" which based on the multilevel step wave modulation strategy. Its principle is the selective elimination of specific harmonics by presetting the appropriate "groove" on the step wave, which can improve the quality of output waveform as well as reduce the output THD. This method is similar to the staircase wave harmonic elimination method, while the only difference is the coefficients of output voltage waveform after the Fourier analysis.

Space Vector Modulation:

Space vector modulation has been widely studied and applied like the two-level SVM; multilevel SVM is a vector based synthesis modulation method. Take a three-phase three-level structure for example, the output voltage of each phase has three kinds of status: P, 0, or N, so the total output of three phase has 27 kinds of status. Its space vector scheme is shown in Fig.5(c). In 27 kinds of status, there are 3 zero vector, 24 non-zero vectors (including 6 vectors whose spatial location are overlapped). So totally there are 19 independent space vectors, which are called the "Basic Vectors". SVM algorithm usually consists of four steps:

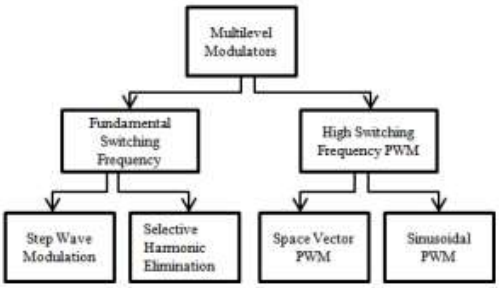
i. Projecting the reference vector into the selected co-ordinate system

ii. Taking the integer value of the projector component.

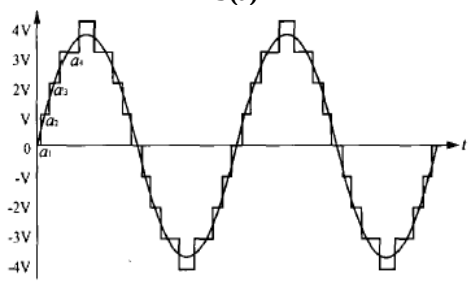
iii. Identifying the neighbouring vector and calculating the operation ratio.

iv. Mapping the switch status.

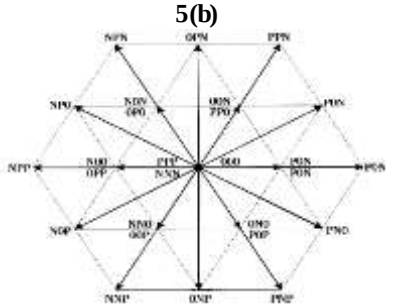
For an M-level inverter, the number of the switching status is m3 and the number of the basic vector is 3m (m-1) +1.



5(a)



5(b)



5(c)

Fig 5 Modulation Strategies (a) classifications of modulation schemes (b) Step wave modulation (c) Space Vector Modulation

Sinusoidal Pulse Width Modulation (SPWM):

The control principle of the SPWM is to use several triangular carrier signals keeping only one modulating sinusoidal signal. For the five level inverter, four triangular carriers are needed (Generally speaking, if a m-level inverter is employed, (m-1) carriers will be needed). The carriers have the same frequency fc and the same peak-to-peak amplitude AC. The zero reference is placed in the middle of the carrier set. The modulating signal is a sinusoid of frequency fm and amplitude Am. At every instant, each carrier is compared with the modulating signal. Each comparison switches the switch "on" if the modulating signal is greater than the triangular carrier assigned to that switches. Obviously, the actual driving signals for the power devices can be derived from the results of the modulating- carrier comparison by means of a logic circuit. SPWM technique can be classified according to carrier and modulating signals. The main parameters of the modulation process are:

1. The frequency ratio k=fc/fn, where fc is the frequency of the carriers and fm is the frequency of the modulating signal

2. The modulation index M=Am / (m *Ac), where Am is the amplitude of the modulating signal, A, is the peak to peak amplitude of the carrier and m'= (m-1)/2 where m is the number of the level which is odd.

Conclusion

The three types of inverters (DCMLI, FCMLI and CCMLI) were designed for a 6.6 kV-12MVA STATCOM and evaluated .It is found that the DCMLI converter had the smallest loss and the CCMLI converter had the highest loss. Even though the FCMLI loss is higher than the DCMLI, the FCMLI is more attractive, because IGBTs of FCMLI have homogeneous loss distribution. Also the cost of DCMLI was the highest; because clamping diodes of DCMLI are expensive. The cost of FCMLI was nearly equal to the cost of CCMLI. From above comparison, it is clear that the FCMLI is the most attractive topology. Reversing Voltage topology has superior characteristics over traditional topologies in terms of the required components as switches, control requirements and reliability. It also requires fewer components. SPWM controller for the inverter also has less complexity and low switching loss. Vector control strategy originates a high-quality load voltage and can work with extremely low switching frequency. The vector control strategy is simple and it can be easily implemented. Novel Multilevel inverter reduces the number of required power switches compared to other traditional topologies.

In modulation schemes Step wave modulation strategy has easy hardware implementation, minimum switching frequency and little switching loss. However, this method would bring a few low order harmonic components into the output waveform, which makes the wave quality poor. Selective Harmonic elimination gives high efficiency, low harmonic content and high utilization of voltage but it has limitation in industrial application due to complicated non- linear transcendental equations that has to be solved when seeking the particular switch points for the multilevel inverter. Space vector modulation has the advantages such as wide range of linear modulation, high DC voltage utilization, little storage space, simple structure, convenient control, easy realization and so on. The calculation work of this SVM Algorithm however increases dramatically with the increase of level number, as well as the algorithm complexity.

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Table I Total Loss and Maximum Tj

	DCMLI	FCMLI	CCMLI
LOSS[KW]	154.5	164.5	184.6
T_j[°C]	114.5	99.6	60.9

Table II Main Unit Cost and Quantities

Main Units Needed	Unit Cost	Quantity		
		DC MLI	FC MLI	CC MLI
IGBT	1.00	48	48	96
Diode	0.74	96	0	0
GDU	0.59	48	48	96
Sensor	0.81	12	12	12
Capacitor[/kJ]	0.10	192kJ	315kJ	164kJ
Heat block [/device]	0.17	48	48	96
Cabinet + Bus Bar + Fan	18.0	5	6	3

Table III Switching states for five level inverters

OUTPUT VOLTAGE V_{xy}	S_1	S_2	S_3	S_4
0	0	1	1	0
$V_{DC}/2$	0	1	0	1
V_{DC}	1	0	0	1