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A new topology on bi-directional ZVS DC–DC converter with phase-shift plus PWM control scheme

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ABSTRACT

A novel phase-shift plus pulse width modulation (PSP) control ZVS bidirectional dc–dc converter is proposed in this paper. By adopting active clamping branch ZVS condition is realized for all switches. The proposed converter has the advantage of wide range of input, output control and reduced switching losses. The performance of proposed converter is compared with the same power rated conventional topology and the results are presented.

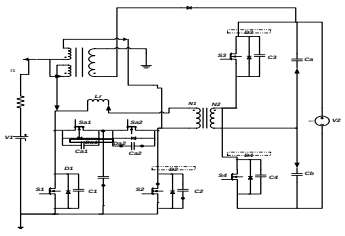
Introduction

With the present energy demand and the enormous potential of nonpolluting renewable energy has attracted the attention of the researchers. However, for effective utilization of these energy resources needs power conversion circuitry. For instance, a DC-DC converter is required for application such as solar systems, electric vehicles, DC uninterruptible power supplies. A bidirectional dc-dc converter is a preferable choice for electric vehicle applications. These converters have the inherent advantages of transferring power in both the directions and the use of high frequency transformers made the converters compact. The converters are broadly classified based on the number of switches used, turn on and turn off methods. Conventionally, the switches are turned ON and OFF with high current and voltage across the switch resulting in increased switching losses and reduced efficiency. However, with the use of Zero voltage switching (ZVS) and Zero current switching (ZCS) the power loss has been substantially reduced in the converter. The ZVS and ZCS techniques are commonly referred as soft switching methods. The demands of a bidirectional dc/dc converter are high frequency, high power density, high efficiency, and high reliability is achieved with soft switched bidirectional converters

For the high power BDC A dual active full bridge dc–dc converter was proposed in [1] and [2], which employs two voltage-fed inverters to drive each side of a transformer. It enables the bidirectional power flow and ZVS for all switches. A dual active half bridge soft-switching bidirectional dc–dc converter was proposed in [3]with reduced power components. However, the current stresses in switches and are asymmetric when the voltage amplitude of two sides of the transformer is not matched, the current stress and circulating conduction loss become higher in [1] - [3]. In addition to that, these converters cannot achieve ZVS in a wide range of load variation while input or output voltage varies. The aforementioned disadvantages make them not suitable for large variation of input or output voltage condition. An asymmetric bidirectional dc–dc converter with PWM plus Phase shift (PPS) control was proposed in [4]. The circulating conduction loss is reduced, however, it results the asymmetric stresses in the main switches and a bias of the magnetizing current which decreases the utilization of the transformer. So, it is not suitable for high power bidirectional conversion. A current-voltage fed PSP ZVS BDC based on current fed half bridge was proposed in [5]. The converter has the advantages of reduced circulating loss and realizes ZVS for wide load variation. The proposed topology is an extended version of the power circuit presented in [5] and it includes a transformer to extend the ZVS range of the switch and to reduce the current stress. Converter is explained in the next section followed by the comparison of the results obtained with both the proposed and conventional method. The conclusions derived are presented in the last section of this paper.

Proposed Topology

The proposed converter with its key waveforms shown in fig.1. It consists of two transformers and total of six switches among them four switches are on the primary side of the main transformer two are on the secondary side of the transformer. The capacitance is provided across each switch to achieve ZVS condition. The operation of the converter is explained with the help of the key waveforms and it comprises of seven modes of operation.



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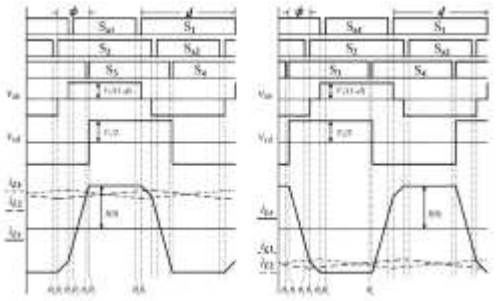
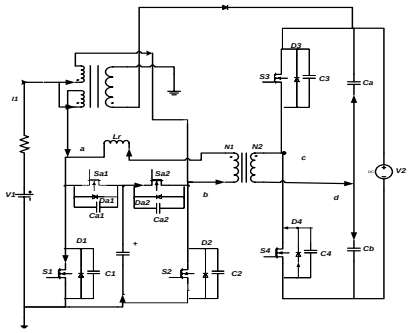


(b) (c)

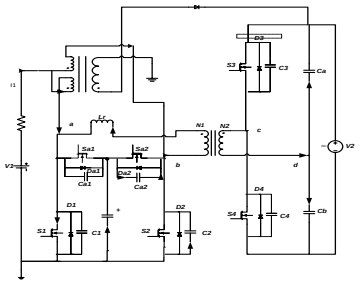
Fig 1.(a) power circuit of conventional bidirectional dc-dc converter.(b) Key theoretical waveforms in (b) Boost mode and (c) Buck mode.

Operation Principle

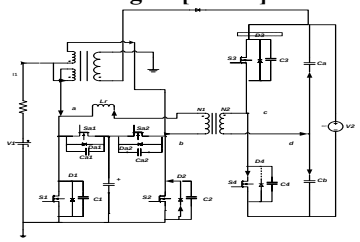
The BDC has two operation modes. It is defined as Boost mode when energy flowing from V_1 side to V_2 side and the counterpart is defined as Buck mode. Before analysis, the following assumptions are given: 1) All the active power devices are ideal switches with parallel body diodes (D_1,D_2,D_3,D_4,D_{a1} andD_{a2}) and parasitic capacitors (C_1,C_2,C_3,C_4,C_{a1} and C_{a2}); 2) The inductance and are large enough to be treated as two current sources with value of value of ;0.5 I_1; 3) The transformer is an ideal one with series leakage inductor. One complete switching cycle can be divided into twelve stages. Because of the similarity, only a half switching cycle is described in detail. As the two sides of the topology are symmetrical, the operation principles in Buck mode are similar to those in Boost mode. The different modes of operations of proposed topology are explained in detail.



Stage 0 [before θ0]

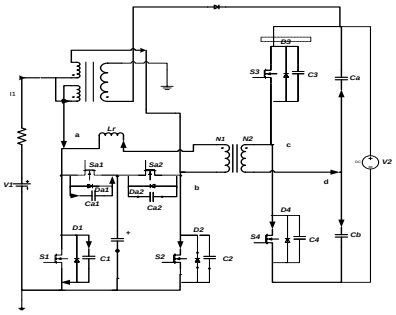


Stage 1 [θ0 θ1]



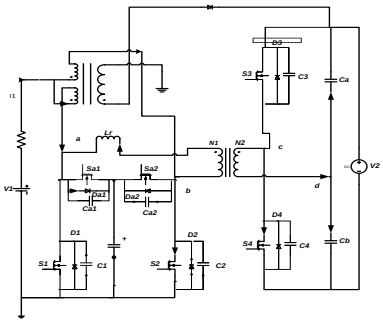
Stage 2 [before θ1 θ2]

Ilr(θ) = -I(0) + N1V2(θ-θ1)/(2N2 Lr)

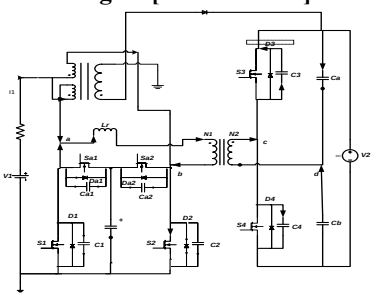


Stage 3 [before θ2 θ3]

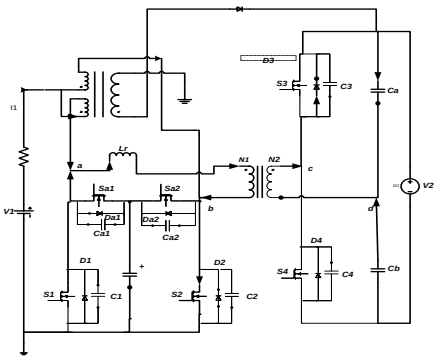
Ilr(θ) = -I(0) + N1V2(2d-1)Π/(2N2ωLr) + N1V2[θ-θ1-(2d-1)Π]/(N2 Lr)



Stage 4 [before θ3 θ4]



Stage 5 [before θ4 θ5]



Stage 6 [before θ5 θ6]

Fig 2: Modes of operation from stage 0 – stage 6

1) Stage 0 [Before θ_0]: S_1, Sa2 and S4 are conducting. At this stage, i_{lr} = -I(0). The power flows from V_1 side to V_2 side.

2) Stage 1 [θ_0, θ1]: At θ_0 , S_{a2} is turned off . L_r ,C_2 and C_{a2} begin to resonate, C_2 is discharged and C_{a2} is charged.

3) Stage 2 [θ_1, θ2]: At θ_1, the voltage across C_2 attempts to overshoot the negative rail. D_2 is therefore forward biased. During this period, S_2can be turned on under zero voltage. The voltage across C_{a2} is clamped at V_{cc} . At this stage,

$$I_{lr}(\theta) = -I(0) + N_1V_2(\theta-\theta_1)/(2N_2\omega L_r)$$

4) Stage 3 [θ_2,θ_3] : At θ_2, S_1 is turned off. L_r , $C_1$and C_{a1} begin to resonate, $C_1$is charged,C_{a1} is discharged. At this stage,

$I_{lr}(\theta)$ = -I(0) + N_1V_2(2d-1)Π/($2N_2\omega L_r$) + N_1V_2[$\theta-\theta_1$-(2d-1)Π]/($N_2\omega L_r$)

5) Stage 4 [θ_3,θ_4] : At θ_3, the voltage across C_{a1} attempts to overshoot the negative rail. D_{a1} is therefore forward biased. During this period, S_{a1} can be turned on under zero voltage. The voltage across C_1 is clamped at V_{cc}. The current of L_r rises to a positive value.

6) Stage 5 [θ_4,θ_5] : At θ_4, S_4 is turned off. L_r , C_3 and C_4 begin to resonate, C_3 is discharged and is C_4 charged.

7) Stage 6 [θ_5,θ_6] : At θ_5, the voltage across C_3 attempts to overshoot the negative rail. $D_3$is therefore forward biased. During this period, S_3 can be turned on under zero voltage. The voltage across C_4 is clamped at $V_2/2$. At this stage, $I_{lr} = I(0)$. The power flows from V_1 side to V_2 side. At θ_6, the second half cycle starts, which is similar to the first half cycle.

The conventional dual active bridge converter with PS control scheme can achieve full control range under soft switching while the amplitude matching of V_{ab} and V_{cd} is naturally matching. However, when the amplitude of V_{ab} and V_{cd} is not matching, the soft switching range is rapidly reduced. By adopting PWM control of $S_1$and S_2, the amplitude matching of V_{ab} and V_{cd} is completely guaranteed in different battery voltage. Therefore, this converter can satisfy well from no load to full load under PSP control. In other words, compared with PS control, PSP control can expand the ZVS range to maximum in entire battery voltage range.

Design Consideration

Converter operation in boost mode:

By proper choice of operating point, transformer winding capacitance can completely replace the external discrete resonant capacitor and the leakage inductance can simply add to the external resonant inductor[6]. The accuracy of the design procedure for high-voltage cases and demonstrates that no snubbing of the transformer windings is required. This is an attractive topology for high-voltage applications. The input and output voltages are listed below.

$V_g = 22\ v, V = 250\ v$, F_s = 100 kHz,

Normalized output voltage is given by

$$M = \frac{V}{N * V_g} = 5.68$$

Normalized output current is given by

$$J = \frac{\frac{N * I}{V_g}}{R_0} = 20.32$$

Normalized frequency is given by

$$F = \frac{f_s}{f_0} = 0.666$$

Where $f_0 = \frac{1}{2 * \pi * sqrt(L * C)} = 15$ MHz

The transformer winding capacitance *C'*, referred to the secondary side, is given by

$$C' = \frac{M * F}{2 * \pi * f_s * \mathbf{V} * \mathbf{J}} = 1nf$$

Output Resistance is given by

$$R_0 = \frac{V_g^2}{I * V} * M * J = 115\ \Omega$$

The tank inductance *L*, referred to the primary side, is given by

$$L = \frac{V_g^2}{2 * \pi * f_s * \mathbf{V} * \mathbf{I}} * M * F * J = 1.1uh$$

The Number of turns of the transformer is given by

$$N = \frac{V}{V_g * M} = 2$$

we can see that the controlling *d* of S_1 and S_2 is to match the amplitude of V_{ab} and V_{cd} . The following equation is satisfied:

$$V_{ab} = \frac{N_1}{N_2} V_{cd}$$

The average voltage of L_1 in one switching period is zero

$V_1 d + (V_1 - V_{ab})(1 - d) = 0$

Further

$V_{cd} = \frac{V_2}{2}$

$$d = \left(1 - 2 * \frac{N_2 V_1}{N_1 V_2}\right) = 0.65$$

3.8 Proposed converter operation in buck mode:

$V_{in} = 250\ v, V_0 = 22\ v$

This class of convertors utilizes the energy stored in the leakage inductance to discharge that stored in the MOSFET switch and transformer capacitances (C_{MOS} and C_{TR}, respectively). Then, the switches are turned on with zero voltage and no power loss or ringing are encountered. Hence, to reduce the switch voltage to zero, there must be enough energy in L_{lk} (which is the result of a certain load current I_o), i.e.

$$\frac{1}{2} L_{lk} \frac{I_0^2}{N^2} > \left(\frac{4}{3} C_{mos} + \frac{1}{2} C_{tr}\right) V_{in} = 0.020747 > 4.166 * 10^{-4}$$

Notice that a nonlinear drain-to-source MOSFET output capacitance is assumed with C_{MOS} being its value at V_{IN}. The factor (4/3) is obtained by computing the total energy stored in a capacitor with square-root voltage dependence. The total capacitance C_B is defined as

$$C_b = \frac{8}{3} C_{mos} + C_{tr} = 1.433 * 10^{-8}$$

$$\frac{L_{lk}}{C_b} > \left(\frac{V_{in}}{\frac{I_0}{N}}\right)^2 = 76.762 > 1.656$$

Examining above two equations reveals that, at a certain critical value of load current *I* , defined as I_{zvs} , the inequality can no longer be satisfied and ZVS is lost. Hence

$$I_{zvs} = N * V_{in} * \sqrt{(C_{\downarrow} b / L_{\downarrow} lk)} = 14.267$$

The point at which ZVS is lost is directly related to an operating impedance of the bridge *Zo* , defined as

$$Z_0 = \frac{N * V_{in}}{I_0} = 1.287$$

Therefore, if a range of load currents ranging from full load down to some percentage of full load is specified for achieving zvs, we may then find a unique value for L_{lk}. Let this range or the ZVS range of load currents be γ , defined as

$$\gamma = \frac{I_{zvs}}{I_0} = 0.1469$$

A ZVS range of γ = 1.0 means that ZVS is attained only at full load and lost at other lighter loads. A value of γ = 0.50

means that ZVS is maintained from full load down to 50% load with ZVS being lost at lighter loads. Notice that it is also possible to design for γ > 1. A value of, say, γ = 1.50 implies no ZVS at any load and that it would be necessary to increase the load 50% beyond its full-load value to achieve ZVS. The parameter y is a distinct characteristic of this topology and has significant effects on its performance and efficiency. These effects are readily determined through overall circuit optimisation. When a value of y is chosen, the required value of leakage inductance is obtained from above equations as

$$L_{lk} = \frac{C_b * z_0^2}{\gamma^2} = 1.1 \text{ uh}$$

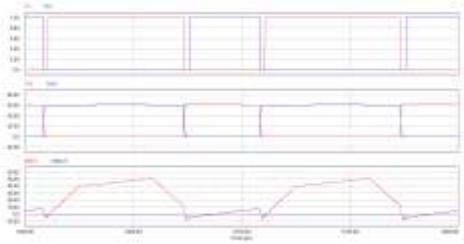
The theoretical value of *N* is given by

$$N = \frac{V_{in}/V_0}{1 + \left(V_{in}/V_0\right) * \frac{k_d}{\gamma^2}} = 2$$

Where $k_d = 4 * f_s * C_b * \frac{V_{in}}{I_0} = 0.0147$

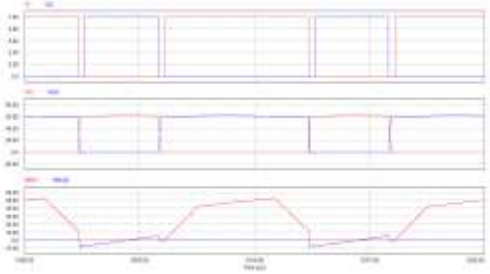
Results

The results shown below are the comparison waveforms of voltage pulses for the switches (S1, Sa1), voltage across the switches (S1, Sa1) and the Current through the switches (S1, Sa1) for both the proposed topology and conventional topology of bi-directional boost dc-dc converter.



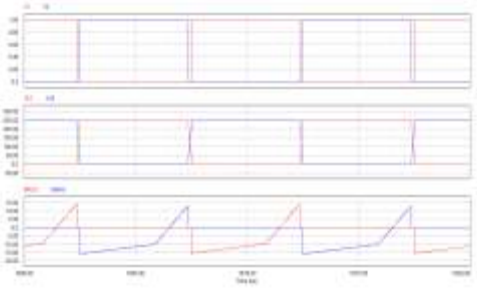
Bi-Directional boost dc-dc converter for V1=22V,V2=250V;.1) Voltage pulses for the switches S1, Sa1; (2) Voltage across the switches S1, Sa1; 3) Current through the switches S1, Sa1.

The results shown below are the comparison waveforms of voltage pulses for the switches (S2, Sa2), voltage across the switches (S2, Sa2) and the Current through the switches (S2, Sa2) for both the proposed topology and conventional topology of bi-directional boost dc-dc converter.



Bi-Directional boost dc-dc converter for V1=22V,V2=250V;1) Voltage pulses for the switches S2, Sa2; (2) Voltage across the switches S2, Sa2; 3) Current through the switches S2, Sa2

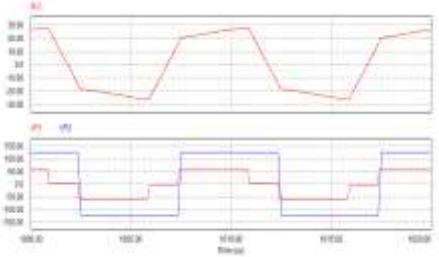
The results shown below are the comparison waveforms of voltage pulses for the switches (S3, S4), voltage across the switches (S3, S4) and the Current through the switches (S3, S4) or both the proposed topology and conventional topology of bi-directional boost dc-dc converter.



Bi-Directional boost dc-dc converter for V1=22V,V2=250V;1) Voltage pulses for the switches S3, S4; (2) Voltage across the switches S3, S4; 3) Current through the switches S3, S4.

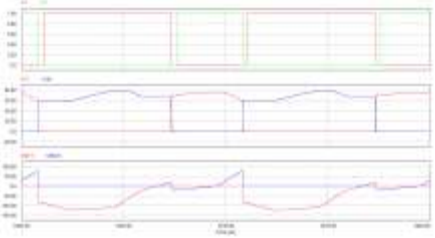
The results shown below are the comparison waveforms of Current through inductor (Lr),

Voltage across primary (VP1) and secondary (VP2) of main transformer for both the proposed topology and conventional topology of bi-directional boost dc-dc converter.



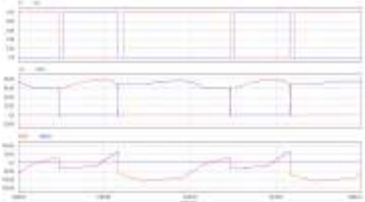
Bi-Directional boost dc-dc converter for V1=22V,V2=250V; (1) Current through inductor (Lr) ,(2) Voltage across primary (VP1) and secondary (VP2) of main transformer.

The results shown below are the comparison waveforms of voltage pulses for the switches (S1, Sa1), voltage across the switches (S1, Sa1) and the Current through the switches (S1, Sa1) for both the proposed topology and conventional topology of bi-directional buck dc-dc converter.



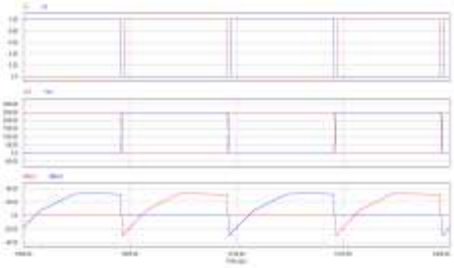
Bi-directional buck dc-dc converter for V1=22V,V2=250V;1) Voltage pulses for the switches S1, Sa1; (2) Voltage across the switches S1, Sa1 ;(3) Current through the switches S1, Sa1.

The results shown below are the comparison waveforms of voltage pulses for the switches (S2, Sa2), voltage across the switches (S2, Sa2) and the Current through the switches (S2, Sa2) for both the proposed topology and conventional topology of bi-directional buck dc-dc converter.



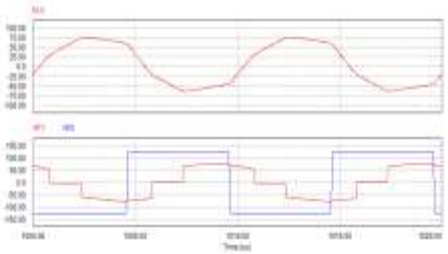
Bi-directional buck dc-dc converter for V1=22V,V2=250V; (1) Voltage pulses for the switches S2, Sa2;(2) Voltage across the switches S2, Sa2 ;(3) Current through the switches S2, Sa2

The results shown below are the comparison waveforms of voltage pulses for the switches (S3, S4), voltage across the switches (S3, S4) and the Current through the switches (S3, S4) for both the proposed topology and conventional topology of bi-directional buck dc-dc converter.



Bi-directional buck dc-dc converter for V1=22V,V2=250V; (1) Voltage pulses for the switches S3, S4; (2) Voltage across the switches S3, S4; (3) Current through the switches S3, S4.

The results shown below are the comparison waveforms of Current through inductor (Lr), Voltage across primary (VP1) and secondary (VP2) of main transformer for both the proposed topology and conventional topology of bi-directional buck dc-dc converter.



Bi-directional buck dc-dc converter for V1=22V,V2=250V; (1) Current through inductor (Lr) ,Voltage across primary (VP1) and secondary (VP2) of main transformer.

Experiment Results And Discussion

The specifications of the converter are given as follows:

1) The battery voltage of V_1 side: V_1 = 22-32 VDC.
2) The rated voltage of V_2 side: 250 VDC.
3) Rated power (P_N): 1.5kW.
4) The turns ratio of the transformer: N_2:N_1 = 2.
5) The leakage inductance of the transformer: Lr = 1.2 μH.
7) The clamping capacitor: Cc = 3μF.
8) The capacitors: Ca = Cb = 470μF.
9) Switching frequency: 100 kHz.

The efficiency is higher in high battery voltage (such as V1=32V, the highest η=0.96 in Boost mode). Unfortunately, the efficiency is lower in low battery voltage (such as V1=22V, the highest η = 0.92 in Boost mode). This degradation is due to the increase of conduction loss with the battery voltage decreases.

Conclusion

A novel ZVS bidirectional dc–dc converter with PS plus PWM control is proposed in this paper, which has the following advantages.

1) All switches realize ZVS in a wide range of load variation while input or output voltage varies.
2) The PS plus PWM control reduces the circulating current.
3) The converter avoids the voltage spike of and with the use of an active clamping branch and .
4) The control strategy realizes energy conversion freely, which has high steady and dynamic performance.

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