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Development of diode clamped inverter based STATCOM using SVPWM technique

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ABSTRACT

This paper presents a Diode Clamped Inverter for Static Compensator (STATCOM) using Space Vector Pulse Width Modulation (SVPWM) technique. Static Synchronous Compensator (STATCOM), a Flexible Alternating Current Transmission Systems (FACTS) controller .For a given dc bus voltage the maximum inverter line-to-line voltage generated by the SVPWM scheme is 15.5% higher than that by the SPWM scheme. SVPWM scheme is used to reduce the switching losses, by changing switching states such that only single phase voltage changes every time. SVPWM strategy enables balancing voltages of the dc capacitors without using additional devices multilevel (three level) inverter is used to reduce THD in its ac output voltages in comparison to the two-level inverter. In order to achieve reactive power control, by maintaining unity power factor at the source end feeding reactive load by three level diode clamped SVPWM Inverter which is adapted as STATCOM is employed in this paper. The control strategy for the compensation is based on the instantaneous active and reactive power theory The STATCOM is modelled and simulated in MATLAB Simulink environment. The simulation results of STATCOM under balance voltage condition are presented.

Introduction

The knowledge of using power electronics devices in transmission network, known as flexible AC transmission systems (FACTS), will enable utility networks to operate like a highly automated, reliable, self correcting and integrated transmission network. Series and shunt compensators are the basic elements of the FACTS controllers. Among those STATCOM is a shunt connected device consists of VSI which is connected to grid through a smoothing reactor. Modern shunt compensators generate /absorb reactive power without energy storage elements like capacitors or inductors [10].

Multi-level diode clamped voltage fed inverters are recently becoming very popular for multi-megawatt power applications with available switching devices [6, 7].The topologies of multilevel converters and application [7] .The main advantage of such an inverter topology is voltage division, i.e., the output voltage is produced through small steps of voltage and the individual switches are submitted only to these small voltage steps.

Three level inverters are employed which more advantages than two level inverters.AC-links have output voltage levels [2] .The blocking voltage of each switch is clamped to the half of DC-link voltage. Performance of multi-level inverter depends on the SVPWM algorithm. A space vector modulation technique is used for the control of a three-phase, diode-clamped converter in both rectifications as well as inversion modes. Space vector pulse width modulation (SVPWM) strategy used to reduce switching loss [2].

STATCOM (Static Synchronous Compensator), with suitable control principle to inject current into the system to compensate both leading reactive power as well as lagging reactive power consumed. In order to increase the power transmission capacity of the line and improves the stability of the power system. The current controlled SVPWM VSI(three-level inverter) based STATCOM is modeled and simulation studies are carried out using mat lab simulation package with a view to maintain the power factor at the source end, feeding capacitive / inductive load. Instantaneous active and reactive power theory [1,8, 9] has been used in developing the control scheme for the STATCOM for maintaining unity p.f at the source end.

Three level diode clamped inverter

The diode clamped multilevel inverter consists of clamping diodes and cascaded dc capacitors to produce ac voltage waveforms with multiple levels. The inverter can be generally configured as a three, four, five or seven-level topology, but only the three-level inverter, regularly known as neutral-point clamped (NPC) inverter.

Mostly, the inverter can be used in the MV drive to reach wide application in high-power medium-voltage (MV) drives. The main features of the NPC inverter include reduced dv/dt and THD in its ac output voltages in compression with two level inverter. On the dc side of the inverter, the dc bus capacitor is divided into two, providing a neutral point Z.

The diodes connected to the neutral point, Dz1 and Dz2, are the clamping diodes. When switches S2 and S3 are turned on, the inverter output terminal A is connected to the neutral point (Z) through one of the clamping diodes. The voltage across each of the dc capacitors is E, which is normally equal to half of the total dc voltage Vd. With a finite value for Cd1 and Cd2, the capacitors can be charged or discharged by neutral current Iz, causing neutral-point voltage deviation.

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Table 1 Switching States

Device switching status (phase A)					
Switching state	S1	S2	S3	S4	Inverter terminal voltage (Vaz)
P	ON	ON	OFF	OFF	E
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	-E

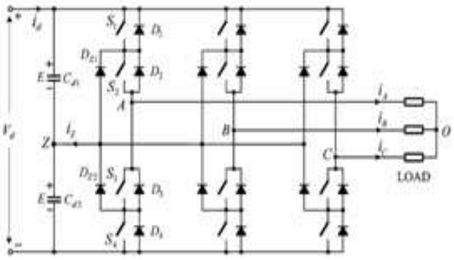

Figure 1. Three level inverter

The circuit of a three-level inverter (Diode-clamped inverter) [3] is shown Figure. 1

Switching states

The operating status of the switches in the diode-clamped inverter can be represented by switching states shown in Table 1. Switching state 'P' denotes that the upper two switches in leg A are on and the inverter terminal voltage V_{AZ}, which is the voltage at terminal A with respect to the neutral point Z, is +E, whereas 'N' indicates that the lower two switches conduct, leading to $V_{AZ} = -E$. Switching state 'O' signifies that the inner two switches S_2 and S_3 are on and V_{AZ} is clamped to zero through the clamping diodes. Depending on the direction of load Current i_A, one of the two clamping diodes is turned on. For instance, a positive load current ($i_A > 0$) forces D_{Z1} to turn on, and the terminal A is connected to the neutral point Z through the conduction of D_{Z1} and S_2.

It can be observed from Table 1 that switches S_1 and S_3 operate in a complementary manner. i.e when one switch is on, the other must be off. Similarly, S_2 and S_4 is also a complementary pair. The gate signals can be generated by PWM, carrier-based modulation, space vector modulation, or selective harmonic elimination schemes. The waveform for V_{AZ} *has* three voltage levels, $+E$, 0, and $-E$. Since there are three levels of voltage, hence it is also called as three level inverter. The inverter terminal voltages V_{AZ}, V_{BZ}, and V_{CZ} are three-phase balanced with a phase shift of $2\pi/3$ between each other. The line-to-line voltage V_{AB} can be found from $V_{AB} = V_{AZ} - V_{BZ}$, which contains five voltage levels ($+2E$, $+E$, 0, $-E$, and $-2E$)

Features of Diode clamped inverter

The three-level Diode clamped inverter provides the following features:

1. No dynamic voltage sharing problem i.e. Each of the switches in the NPC inverter can with stand only half of the total dc voltage during commutation.
2. Static voltage equalization without using additional components. This(static voltage equalization) can be achieved when the leakage current of the top and bottom switches in an inverter leg is selected to be lower than that of the inner switches Low THD and dv/dt in comparison with the two level inverters.

Causes of neutral-point voltage deviation

Due to the influence of small and medium voltage vectors neutral point voltage may be affected.

1. Unbalanced dc capacitors due to manufacturing tolerances
2. Inconsistency in switching device characteristics
3. Low THD and dv/dt in comparison with the two level inverters

SVPWM Technique

Space vector concept

The concept of space vector is derived from the rotating field of AC machine which is used for modulating the inverter output voltage. In this modulation technique the three phase quantities can be transformed to their equivalent 2-phase quantity either in synchronously rotating frame (or) stationary frame. From this 2-phase component the reference vector magnitude can be found and used for modulating the inverter output. The process of obtaining the rotating space vector is explained in the following section, considering the stationary reference frame. Each leg of the DCI can solely take three different switching states. Consequently the DCI has twenty seven valid switching states(3^3)[5]. Each switching state is denoted with a three letter code (e.g. PNN, POP) which corresponds to the three nodes (a, b,c), respectively, then being connected to the positive (P), zero (0) or negative (N) dc rail.

The principle of the SVM is that we use these switching states to compose the desired output voltage.

Every switching state corresponds to specific output voltages which are equivalent to a vector on an α-β plane, using

$$\begin{bmatrix} V_\alpha \\ \\ V_\beta \end{bmatrix} = \begin{bmatrix} \frac{3}{2} & 0 & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

Some switching states are equivalent to the same vector as they match up to the same output voltages. Therefore the switching vectors are only nineteen, as shown in fig. and can be divided into four types: zero vectors (V_0) of magnitude zero , short vectors (V_1 to V_6) of magnitude V_d /3, medium vectors (V_7 to V_{12}) of magnitude $\sqrt{3}V_d/3$ and large vectors (V_{13} to V_{18}) of magnitude $2V_d/3$.The voltages that we want to generate at the output of the inverter can also be matched to a reference vector Vref on an α-β plane.

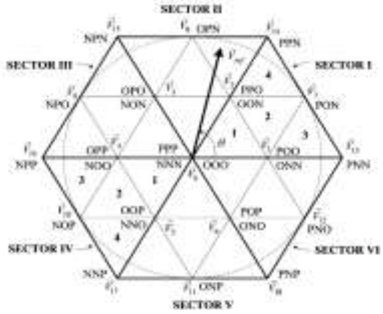

Figure 2. Division of sectors and regions

SVM can be divided into the following three steps:

1. Selection of switching vectors.
2. And computation of the duty cycles of the selected switching vectors.
3. Then Selecting Switching states

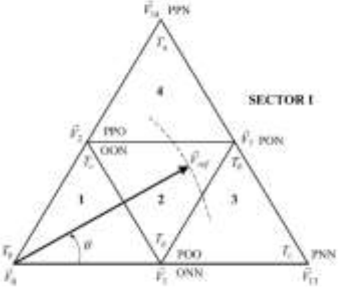

Figure 3.Vector voltages and Dwell times

Dwell time calculation

To facilitate the dwell time calculation, the space vector diagram of Figure. (2) can be divided into six triangular sectors (I to VI), each of which can be further divided into four triangular regions (1 to 4) as shown in Figure. 3. SVM algorithm for the NPC inverter is based on “volt-second balancing” principle. The product of the reference voltage V_{ref} and sampling period Ts equals the sum of the voltage multiplied by the time interval of chosen space vectors. In the NPC inverter, the reference vector V_{ref} can be synthesized by three nearest stationary vectors. For instance, when V_{ref} falls into region 2 of sector I . The three nearest vectors are V_1, V_2, and V_7, from which

$$V_1 T_a + V7\ T_b + V_2 T_c = V_{ref} Ts \quad (1)$$

$$T_a + T_b + T_c = T_s \quad (2)$$

where T_a, T_b, and T_c are the dwell times for V_1, V7, and V_2, respectively. Note that V_{ref} can also be synthesized by other space vectors instead of the nearest three.

Statcom Principle

The basic principle of reactive power generation by a voltage source inverter is same as the conventional rotating synchronous machine. The basic voltage source converter scheme for reactive power generation is shown, in the form of a single line diagram in Figure. (4).Shunt and series compensators are the basic elements of the FACTS controllers. Among those statcom is a shunt connected device.

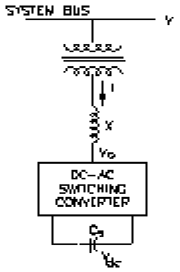

Figure 4 Single line diagram of Statcom

From a dc input voltage source, provided by the charged capacitor Cs, the converter produces a set a controllable three-phase output voltages with the frequency of the ac-power system. Each output voltage is in phase with and coupled to the corresponding ac system voltage via a relatively small tie reactance (0.1 - 0.15 p.u) coupling. The magnitude and direction of the reactive current, I shown in Figure 4 is determined by the magnitude of the system voltage, magnitude of the converter output voltage and reactance, is given by equation (3).

$$Q = \frac{1 - \frac{E}{V}}{X} V^2$$

$$I = \frac{V - E}{X} \quad (3)$$

The corresponding reactive power Q exchanged is given by equation (4).

(4)

From the above equation, it is clear that by varying amplitude of the converter output voltages produced, the reactive power exchange between the converter and the ac system can be controlled. If the amplitude of converter voltage is more than the ac system voltage, the leading VARs is produced. Similarly if the amplitude of the converter voltage is lower than the ac system voltage, lagging VARs is produced. If the amplitude of the output voltage is equal to that of the ac system voltage, the reactive power exchange is zero.

Statcom Control Circuit

SVPWM converter based STATCOM can be used to supply the required reactive power to transmission line with a view to maintain constant voltage at the point of connection (PCC) or maintain the power factor at a required value. In this paper a controlling scheme for STATCOM which is connected at the load end of a three-phase distribution and transmission network, is developed and modeled to maintain unity power-factor at the source end. The control circuit monitors the reactive power consumed by the load and accordingly controls the output current of the SVPWM converter (in directly controls the magnitude and phase angle of output voltage of the converter) to maintain unity power factor at the source end.

Reactive power control circuit as described here is developed using active and reactive power theory instantaneously [1]. The better response to the VAR (reactive power) demand can be achieved with the voltage sourced svpwm converter as it operates at higher switching frequency. Hence before going into the details of control circuit description, here is brief explanation of the user defined models

Voltages and currents at the load end are measured and are converted to control level signals by using an in-built matlab simpower modules.

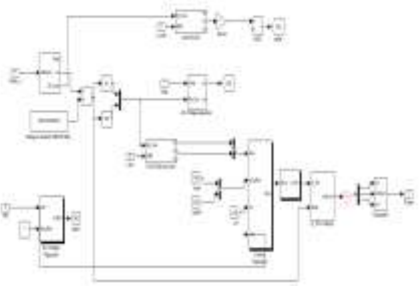

Figure 5. Statcom control circuit

The currents and voltage signals at control level are fed to the three-phase to two-phase conversion block. These voltage and current signals in □ - □ co-ordinates are fed to the two-phase to power block. This block gives the equivalent active power and reactive power, i.e. load active power and reactive power. The inverter should generate reactive power of the same magnitude as the reactive power consumed by the load to make to reactive power supplied by the source is zero and thereby to maintain unity power factor at the source end.

In our convention, if the system absorbs reactive power of amount q, then it is +q and if it generates reactive power of amount q, then it is -q. Therefore it the load absorbs the reactive power of amount q, then it is +q. So, the reference reactive power for inverter which is to be generated by it, is -q. This -q is obtained with the help of gain block (with K = -1). For the closed loop control, the reactive power generated by the inverter has to be calculated instantaneously. This reactive power can be calculated in the same way as described above by feeding the inverter output voltages and currents supplied by the inverter.

The reactive power supplied by the inverter is subtracted from the reference reactive power to obtain the error in reactive power. The error signal is passed through a PI- controller to obtain the reactive power signal (q^*) which is fed to power to two phase current conversion model. This conversion model requires a active power signal, reactive power signal and voltages at which converter is connected to grid in α - β co-ordinates as inputs. In an independent dc source fed converter the input active power signal to the power to the two-phase current conversion model is zero as there is no need to take active power from the grid. Whereas the active power signal should be obtained from a dc bus voltage controller in case of a self-controlled dc bus fed converter as the dc bus has to meet the switches losses in the converter. The outputs of power to two-phase current conversion model gives reference currents ($I\alpha$,$I\beta$) in α-β co-ordinates.

These reference currents are converted into equivalent three phase reference currents (I_a, Ib, Ic) by the two-phase to three-phase model. The converter should generate these reference currents to change the magnitude and phase angle of the converter voltage to maintain the unity power factor at the source end and also to maintain dc capacitor voltage at the required value.

The inverter output current should be controlled is a closed-loop, so that the output currents of the inverter closely matches the reference currents. For realizing a closed loop current controlled voltage source converter, the reference current of each phase is compared with respective converter phase current and this error is processed through PI controller.

Simulation Results For Three-Level Inverter

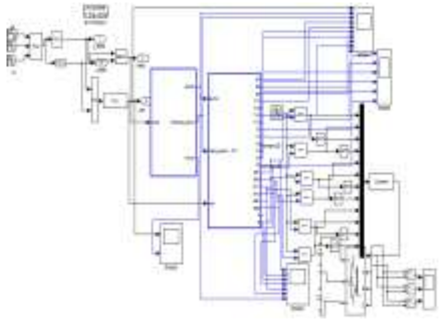

Figure 6. Switching vectors of three-level inverter

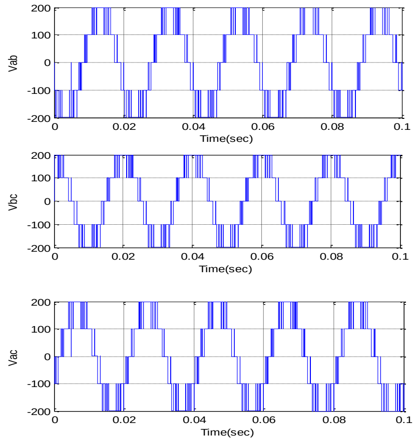

Figure 7. Three level output voltage using SVPWM technique

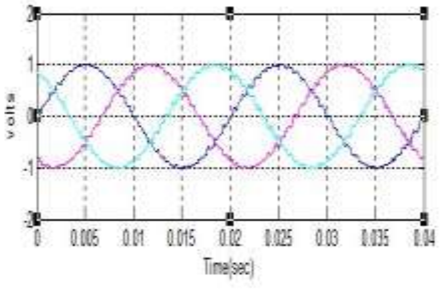

Figure 8. Voltage source with compensation

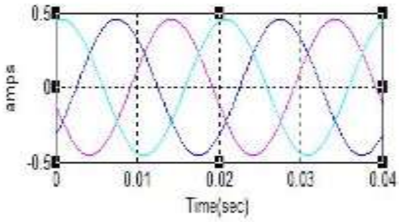

Figure 9. Source Current without compensation

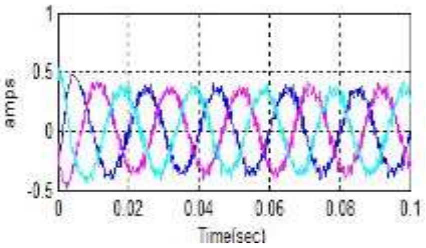

Figure 10. Source current with compensation

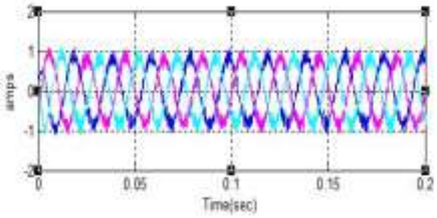

Figure 11. STATCOM current

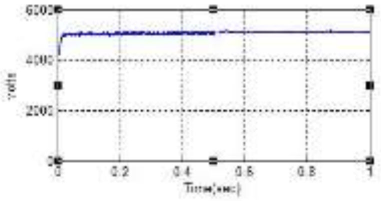

Figure12. DC link voltage

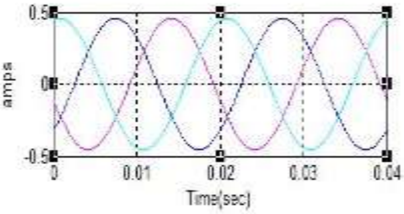

Figure 13. Voltage source without compensation

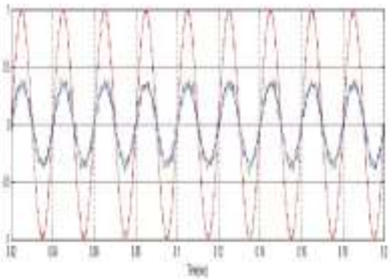

Figure 14. Voltage source with compensation having voltage and current in phase

Conclusion

SVPWM converter based STATCOM has been simulated on the basis of instantaneous active and reactive power theory, using Matlab simulation package. The operation of the STATCOM is verified with the system connected to a simple transmission line feeding R-L/R-C load. The output current of the SVPWM converter is controlled indirectly controls the magnitude and phase angle of the output voltage of the converter to maintain unity power factor at the source end feeding R-L / R-C load.

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