Available online at www.elixirpublishers.com (Elixir International Journal)

Electrical Engineering

Elixir Elec. Engg. 38 (2011) 4339-4342

ISSN: 2229-712X

Analysis and simulation of multilevel inverter system

G. Mahesh Manivanna Kumar[1] and S. Rama Reddy[2]

[1]Department of Electrical and Electronics Engineering, Sathyabama University, Chennai

[2]Department of Electrical and Electronics Engineering, Jerusalem Engineering College, Chennai.

ARTICLE INFO

Article history:

Received: 22 August 2011;

Received in revised form:

26 August 2011;

Accepted: 31 August 2011;

Keywords

Neutral point clamped inverter,

Cascaded multi level inverter,

H-bridge inverter.

ABSTRACT

This paper deals with the simulation of three, five, seven and nine level output using H-bridge inverter. This paper presents H – bridge inverter simulated using MATLAB with different levels (like three, five, seven and nine level). The percentage (%) total harmonic distortion THD is calculated. The harmonic reduction is achieved by selecting appropriate switching angles. The functionality verification of the three level, five level, seven level and nine level output is done using MATLAB.

Introduction

The multilevel inverter was first introduced in 1975. The three level converters the first multilevel inverter introduced. A multilevel converter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs. With increasing number of dc voltage sources, the converter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency-switching scheme. The primary advantage of multilevel inverter is their small output voltage, results in higher output quality, lower harmonic component, better electromagnetic compatibility, and lower switching losses [2].

Multilevel inverter includes an array of power semiconductors and capacitor voltage sources, the output of which generates voltages with stepped waveforms with less distortion, less switching frequency, higher efficiency, lower voltage devices and better electromagnetic compatibility [4]. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltages at the output, while the power semiconductors must withstand only reduced voltage.

Bridge Inverter

Three Level Mode

Another characteristic is that the "H" topology has many redundant combinations of switches' positions to produce the same voltage levels. As an example, the level "zero" can be generated with switches in position S(1) and S(2), or S(3) and S(4), or S(5) and S(6), and so on [7] [8] [9].

Another characteristic of "H" converters is that they only produce an odd number of levels, which ensures the existence of the "0V" level at the load .For example, a 51-level inverter using an "H" configuration with transistor-clamped topology requires 52 transistors, but only 25 power supplies instead of the 50 required when using a single leg [8]. Therefore, the problem related to increasing the number of levels and reducing the size and complexity has been partially solved, since power supplies have been reduced to 50%. Fig 1.a shows the circuit diagram of H-bridge inverter operated in three level output mode.

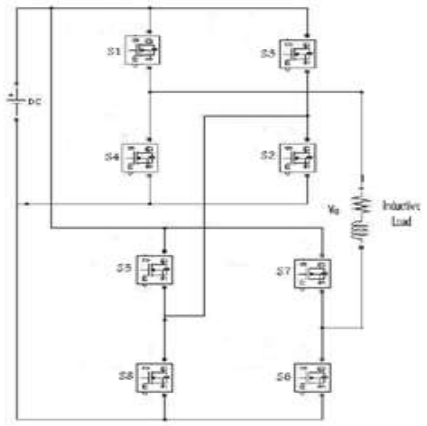

Fig 1a H-Bridge Inverter for Three Level Output Mode

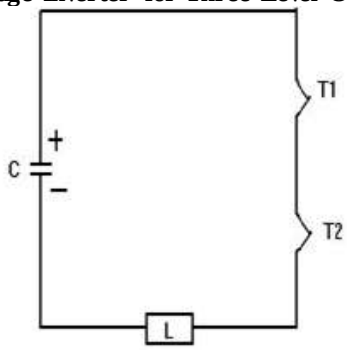

Fig1b. Mode-I (Vout = Vdc/2)

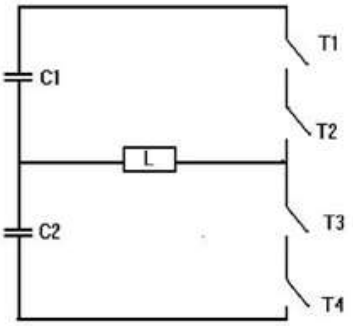

Fig. 1.c Mode-II (Vout = 0)

Tele:

E-mail addresses: maheshmanivannakumarg@yahoo.co.in

The mode of operation of H-bridge inverter operated in three level output has been explained based on the line diagram as shown in fig 1.b, 1.c, 1.d and 1.e. During mode 1, switches T1 and T2 are turned on, the voltage level of the the output voltage Vout = Vdc/2. During mode 2, switches T1, T2, T3 and T4 are turned off, the voltage level of the output voltage Vout = 0. During mode 3, switches T3 and T4 are turned on, the voltage level of the output voltage Vout= -Vdc/2. During mode 4, the switches T1, T2, T3 and T4 are turned off, the voltage level of the output voltage is Vout = 0. Table.1shows the switching sequence of H-bridge operated in three level output mode.

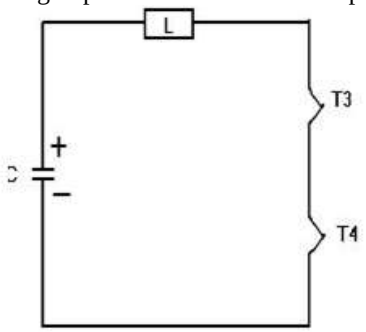

Fig. 1.d. Mode-III (Vout = -Vdc/2)

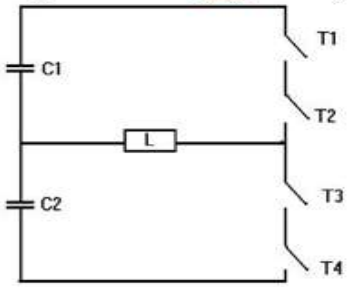

Fig. 1.e. Mode-IV (Vout = 0)

Fig 2. Shows the circuit diagram of H-bridge inverter operated in five and seven level output mode. The upper bridge is main inverter and the lower bridge is auxiliary inverter.

The ac terminal voltages of each bridge are connected in series. Unlike the diode clamp or flying capacitors inverter, the cascaded inverter does not require any voltage-clamping diodes or voltage balancing capacitors. This configuration is useful for constant frequency applications such as active front-end rectifiers, active power filters, and reactive power compensation.

In this case, the power supply could also be voltage regulated dc capacitor. The circuit diagram consists of two cascade bridges. The load is connected in such a way that the sum of output of these bridges will appear across it. The ratio of the power supplies between the auxiliary bridge and the main bridge is 1:2 for seven level and 1:3 for nine level output. One important characteristic of multilevel converters using voltage escalation is that electric power distribution and switching frequency present advantages for the implementation of these topologies [9].

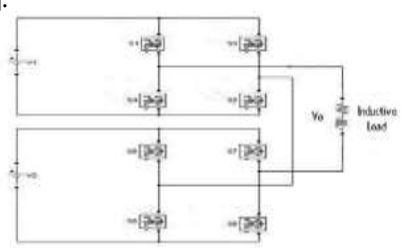

Fig 2. H-Bridge Inverter for five and seven Level Output Mode

Using H-Bridge inverter the harmonics are reduced in 3 and 7 level output voltages. The inverter generates a high quality output voltage waveform. It reduces dv/dt stress imposed on power switching devices and also harmonic components of output voltage and load current quite well. Table.2 shows the switching sequence of H-bridge operated in seven and nine level output mode.

The phase output voltage is synthesized by the sum of two inverter outputs. Each inverter bridge is capable of generating three different levels of voltage outputs. The main bridge can generate +3Vdc, 0, -3Vdc and the auxiliary bridge can generate +Vdc, 0, -Vdc. By using appropriate combinations of switching devices many voltage levels are obtained.

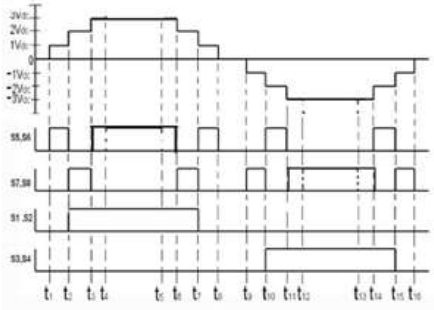

Fig .3 Switching waveform of H-Bridge Inverter for seven Level Output Mode

When the positive group switches are turned on the voltage across that particular bridge is positive. When the negative group switches are turned on the voltage across that particular bridge is negative. When S1, S2 are turned on the voltage across the main bridge is +3Vdc. Fig 3 shows the switching sequence waveform of seven level inverter.

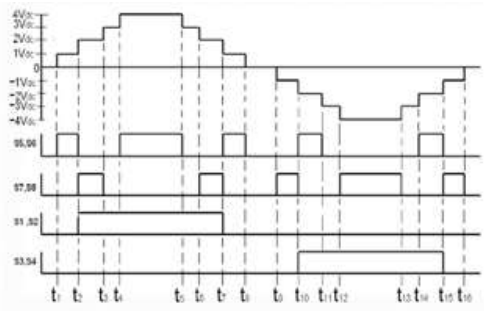

Fig .4 Switching waveform of H-Bridge Inverter for nine Level Output Mode

Harmonic Reduction

To eliminate 5th, 7 th, and 9th order harmonics, the firing angles for each level is found by solving the following equations.

$Cos\ 5a_1 + Cos\ 5a_2 + Cos\ 5a_3 + Cos\ 5a_4 = 0$

$Cos\ 7a_1 + Cos\ 7a_2 + Cos\ 7a_3 + Cos\ 7a_4 = 0$

$Cos\ 9a_1 + Cos\ 9a_2 + Cos\ 9a_3 + Cos\ 9a_4 = 0$

Using Math CAD, the values of the "a" is obtained as follows

a_1 = 12.834 degree a_2 = 29.908 degree a_3 = 50.993 degree a_4 = 64.229 degree

a_1, a_2, a_3, a_4 is the switching sequence of T_1, T_2, T_3 and T_4 respectively. where a_1, a_2, a_3, a_4 are the firing angles in degrees. The switching instants are obtained by carrying out the above calculations.

Simulation Results of H – Bridge Inverter

H – bridge is operated in three level mode simulink circuit shown in fig 5.a. The output of the H – bridge inverter is connected with inductive load. The H – bridge inverter converts the DC voltage into AC voltage in various steps. The switching

strategy of the circuit has explained in the previous section. This circuit is simulated in MATLAB and the output wave form and harmonics by FFT analysis is obtained. The output waveform is shown in the fig 5.b and 5.c shows the harmonics represent in the output. The THD value is 10.15 %.

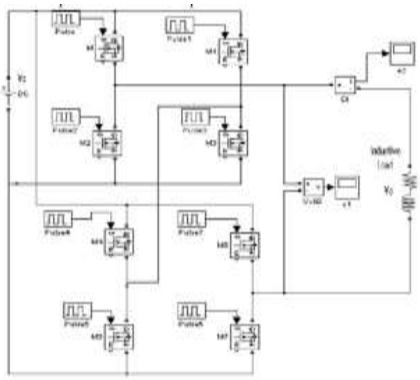

Fig. 5.a. Simulink Circuit for H – Bridge – 3 level output

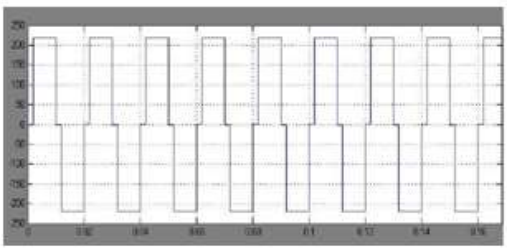

Fig. 5.b. H – Bridge – 3 level mode output voltage

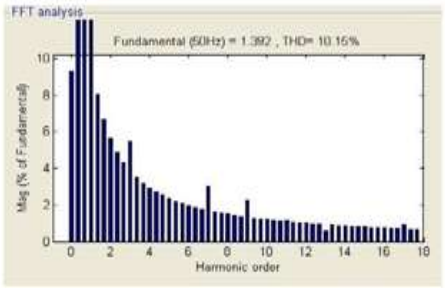

Fig. 5.c. H – Bridge – 3 level mode FFT analysis

H – bridge inverter is operated in five level output mode simulink circuit shown in fig 6.a. The output of the H – bridge inverter is connected with RL load. The H – bridge inverter converts the DC voltage into AC voltage in various steps. The switching strategy of the circuit has explained in the previous section. This circuit is stimulated in MATLAB and the output waveform and harmonics by FFT analysis is obtained. The output waveform of both pure resistive and inductive load is shown in the fig 6.b and 6.c. The output current waveform of the H – bridge inverter in five level mode with inductive load shown in fig 6.d. Fig 6.e shows the harmonics represent in the output. The THD value is 16.45 %.

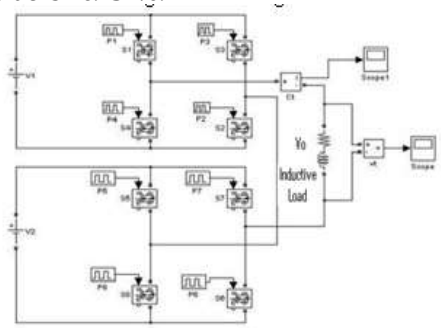

Fig.6.a. simulink circuit of H – Bridge 5, 7 and 9 – Level output mode

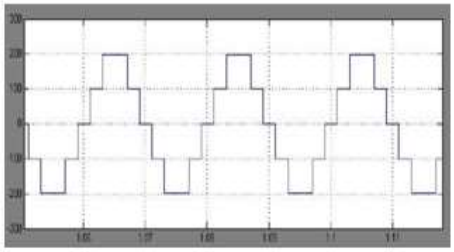

Fig. 6.b H – Bridge 5 – Level Inverter output voltage with R load

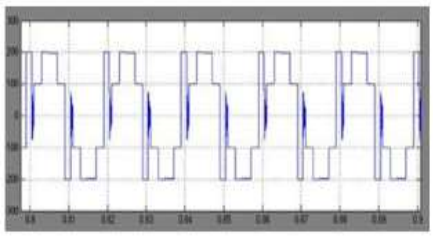

Fig. 6.c H – Bridge 5 – Level Inverter output voltage with RL load

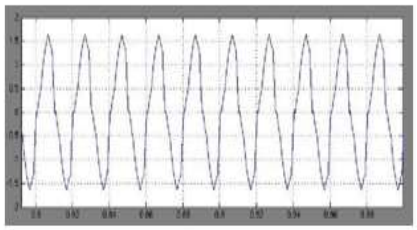

Fig.6.d H – Bridge 5 – Level Inverter output current with RL load

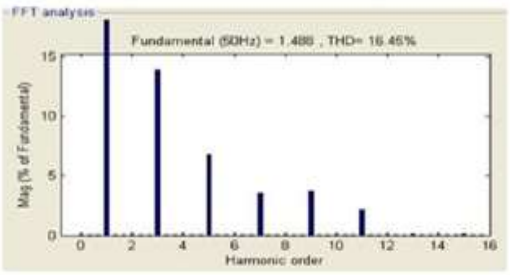

Fig. 6.e H – Bridge 5 – Level Inverter FFT analysis

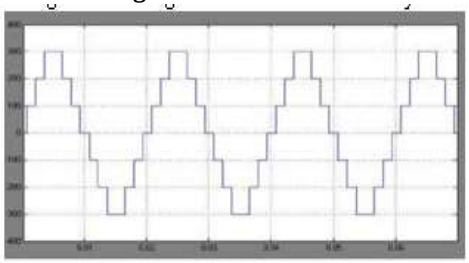

Fig. 7.a H – Bridge 7 – Level Inverter output voltage

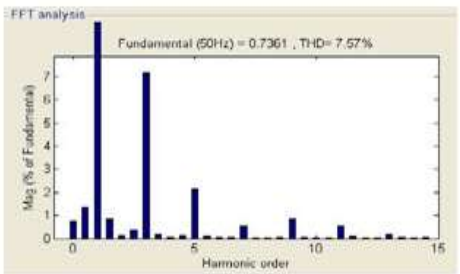

Fig. 7.b. H – Bridge 7 – Level Inverter FFT analysis

H – bridge inverter is operated in nine level output mode simulink circuit as shown in fig 6.a. The output of the H – bridge

inverter is connected with inductive load. The H – bridge inverter converts the DC voltage into AC voltage in various steps. The switching strategy of the circuit has been explained in the previous section. This circuit is simulated in MATLAB and the output wave form and harmonics by FFT analysis is obtained. Fig 8.a shows the switching pulses of nine level inverter. The output voltage and output current waveform of inductive load shown in the fig 8.b and 8.c. Fig. 8.d shows the harmonics represent in the output. The THD value is 6.34 %.

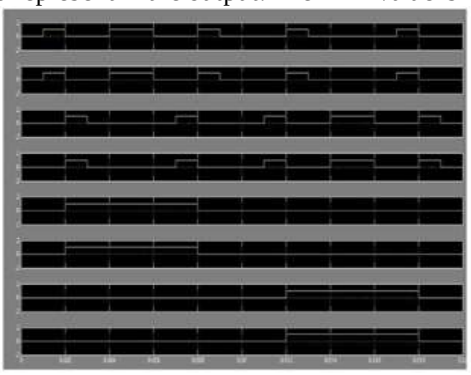

Fig.8.a H – Bridge 9 – Level Inverter individual switching pulse

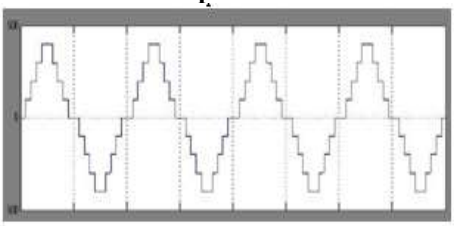

Fig.8.b H – Bridge 9 – Level Inverter output voltage

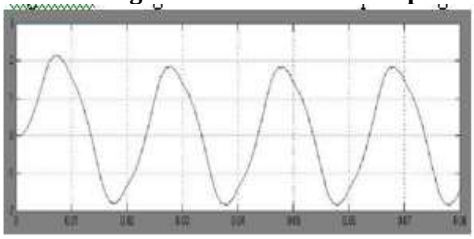

Fig.8.c H – Bridge 9 – Level Inverter output current

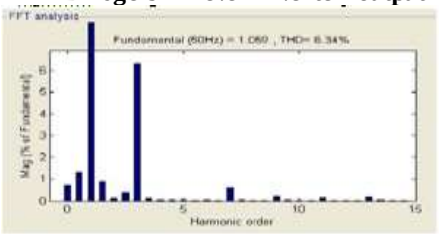

Fig.8.d H – Bridge 9 – Level Inverter FFT analysis

The THD obtained from various circuits are compared. It can be found from table 3 that with the use of H-Bridge three level inverter the THD level is 10.15%. Further with the use of H-Bridge five level inverter the value of THD is 16.45% and seven level inverter the %THD are 7.57 %. While H bridge inverter is operated in the nine level output mode the %THD level is drastically reduced to 6.34%. This shows an improved performance of the H-bridge inverter.

Conclusion

The H-bridge inverter is simulated in different levels of mode with reduced harmonics. Finally the harmonics in multilevel inverter at different stages are compared. From the comparison, it can be seen that the H-bridge inverter operated in nine level output mode has least value of THD.

Acknowledgment

The authors acknowledging the support given by power electronics division, Sathyabama University, Chennai for conducting the experimental studies May 2006 to April 2011.

References

[1]John N. Chiasson, Leon M. Tolbert, Keith J. McKenzie, Zhong Du, " A Complete solution to the harmonic elimination problem", IEEE transactions on power electronics, Vol. 19, No.2, pp. 491-498, March 2004

[2]Jose Rodriguez, Jin-Sheng Lai and Fang Zheng, "Multilevel Inverters: A survey of topologies, Control applications," IEEE transactions on Industrial Electronics, Vol.49, No. 4, pp. 724-738, August 2002

[3]V. G. Agelidis and M. Calais, "Application specific harmonic performance evaluation of multicarrier PWM techniques," in proc. IEEE PESC'98, vol. 1, 1998, pp. 172 – 178.

[4]A. Nabae, I. Takahashi, and H. Akagi, " A new neutral-point-clamped PWM inverter, " IEEE Trans. Ind. Applicat., vol. IA – 17, pp. 518 – 523, Sept./Oct. 1981.

[5]P. D. Ziogas, "Optimum voltage and harmonic control PWM techniques for three-phase static UPS inverters," IEEE Trans. Ind. Applicat., vol. IA-16. no. 4, pp. 542-546, July/Aug. 1980.

[6]H. Patel and R. G. Hoft, " Generalized techniques of harmonic elimination and voltage control in thyristors: Part – I Harmonics elimination," IEEE Trans. Ind. Applicat., vol. IA-9, no. 3, pp. 310-317, May/June 1974.

[7]E. Babaei, S. H. Hosseini, G. B. Gharehpetian, M. T. Haque, and M. Sabahi, "Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology," Elsevier J. Electr. Power Syst. Res., vol. 77, no. 8, pp. 1073–1085, Jun. 2007.

[8]M. Manjrekar, P. K. Steimer, and T. Lipo, "Hybrid multilevel power conversion system: A competitive solution for high-power applications," IEEE Trans. Ind. Appl., vol. 36, no. 3, pp. 834–841, May/Jun. 2000.

[9]Z. Du, L. M. Tolbert, J. N. Chiasson, and B. Ozpineci, "A cascade multi-level inverter using a single dc power source," in Proc. IEEE APEC, 2006, pp. 426–430.