

Available online at www.elixirpublishers.com (Elixir International Journal)

# **Advanced Engineering Informatics**



Elixir Adv. Engg. Info. 39 (2011) 4576-4578

# Routing in communication network using VLSI technology

N.J.R. Muniraj

ABSTRACT

Tejaa Shakthi Innovation Centre, Tejaa Shakthi Institute of Technology, Coimbatore.

# ARTICLE INFO

Article history: Received: 15 July 2011; Received in revised form: 18 September 2011; Accepted: 25 September 2011;

# Keywor ds

Topology, Routing, Leonardo spectrum. In recent years communication network has been undergoing major changes in network architecture and services. Network must be designed for flexibility and adaptability with respect to access topology and routing. The system should operate well under the variety of unexpected condition and node failures. Under such situation the shortest path table must be updated properly. Many traditional algorithms were used has several drawbacks. In order to resolve that drawbacks, a New VLSI based routing network model is proposed for routing which can handle component failures. The learning algorithm for routing is developed using cost function to be minimized to find the optimized path. It is simulated and synthesized using Verilogpro and Leonardo spectrum. Also it has been analyzed using c.

#### © 2011 Elixir All rights reserved.

## Introduction

In recent years, communication networks have been undergoing major changes in network architecture and services. These changes have provided challenges for network planners for use information age technologies to achieve their objectives. Network must be designed for flexibility and adaptability with respect to access topology, routing and demand patterns. In particular, the system should operate well under a variety of unexpected conditions and recover quickly from component failures. In the network design, its performance can be measured by the network reliablity or the transmission delay by assuming no component failures. But if failures happen, as they always do the operation of the network does not stop. It continues to operate at a degraded level of service. Under such situation, the information of shortest path table must be upgraded by reconsidering the new state of network. Many traditional algorithms have been proposed to look for the optimal or suboptimal routes. However, there are several drawbacks for these approaches. First, the computations are massive in finding the optimal route. Second the speed of finding new routes cannot respond fast enough to the situation, when unreliable components fail. Third, the components failure of one node usually influences other nodes. VERILOG HDL is esteem software, which is used for practical circuit implementation, is especially a single chip designer. The efficient and extremely powerful method described here could be practically implemented. Simulated and synthesized results can be shown during the presentation of paper.

## Path Determination and Packet Switching

The path determination function enables a router to evaluate the available paths to a destination and to establish the preferred handling of a packet. Routing services use Network topology information when evaluating network paths. The information can be configured by static or dynamic process.

The Routing algorithm provides best effort end-end packet delivery across inter-connected networks. It uses Routing updates to send packets from source network to destination network. After Router determines which path to use, it proceeds with forwarding packet. It takes the packet that it accepts on one interface and forwards it to another interface that reflects the best path to the packets destination.

To be practical, a network must consistently represent the paths available network routers. Each path between the routers has a number that router use as network capacity or link capacity. Greater the link capacity and lesser the cost function will be chosen best path for switching a packet. The switching function allows a router to accept a packet on one interface and forward it through a second interface. The path determination function allows a router to select a most appropriate interface for forwarding a packet.

# Types of Switching The Packet

- Circuit switching
- Packet switching
- Circuit switching:

Circuit switched connections are a WAN switching method. This means that a dedicated circuit is created through a carrier network during call setup and destroyed during call tear down. The most commonly used form of this type of communication is your telephone. Call setup happens when you pick up the phone and call a friend, while call tear down is what happens when you hang up.

## Packet switching:

Packet switched Networks are not so much a WAN connection as they are WAN service. There is no end-to-end physical connection. Instead they must use a virtual circuit through a public data network (PDN) to communicate with remote sites. These PDN's typically use the first three layers of OSI model to move your data on its own internal network. Your router has no idea how many different networks it takes to get through the public network. Packet switching networks use statistical multiplexing techniques to control network access. It works dynamically enable the sharing of network medium. This type of connection tends to cost effective.

#### **Routing Algorithm**

Routing loop can occur if a network slow convergence on a configuration causing inconsistent routing entries. When the topology of Internet work changes, routing table updates must occur very fastly. When it doesn't occur properly the problem of routing loop may occur.

4576

Due to wrong information in the routing table, the packet switches from one router to another without moving to the destination. And it must continuously and the movement of routing packet may count to infinity.

The communication network is usually modeled by a stochastic graph G = (V, E) where E, V are the sets of nodes (Vertices) and links (Edges) of G. Before stating a problem, we first define certain parameters and their properties. These notations are as follows.

- S => Source node
- t => destination node
- n => no. of nodes in the destination topology of the network
- $h \Rightarrow$  the max. no. of links of optimal path s to t

By definition, h cannot be greater than n-1 their layer h, the more possible alternate paths may be obtained. However paths do not exists when h is smaller than minimum no. of links in all possible paths.

The link capacity s defined to be maximum traffic flow that a link can support. An N-by-N matrix C is used to represent the link capacity between each pair of nodes. The value Cij stands for the capacity.

The above algorithm can be implemented using C language and VLSI Technology. Because of adaptability, easy replacement, miniature in size, place & route we go for VLSI technology.

# Flow Chart:



#### Simulation: Result 1:



**Result 2:** 



#### **Result 3: (Using C)**

Fixed path routing

Multi path routing

Enter your choice  $[1 \text{ or } 2] \rightarrow 1$ 

Enter the source and destination  $\langle s,d \rangle 3,10$ 

From the node 3 to node 10 there are 16 paths, they are as follows:

Press any key to continue The best path is: 3 - 7 - 10And the cost is 1622.500000 The best path is: 3 - 7 - 10



Program ands here!

#### **Conclusion:**

In this paper a new VLSI routing network model has been proposed to solve the routing problem of communication network with failure components. The results obtained using VLSI technology shows that the problem of routing can successfully be solved. Using illustrative examples of 17-node network, the effectiveness of this algorithm is demonstrated. The above results are simulated and synthesized using VLSI technology and it can be further improved. At the time of presentation it will be explained.

#### **References:**

1. Thomas, Golding, Van Oene, Coker, Newcomb, Mason, Quiggle, "Interconnecting Cisco Network Devices", Tata McGraw Hill 2001.

2. J. Bhaskar "Verlog Primer."

3. Puckellnel. D. A and Eshraghain. K, "Basic VLSI Design "PHI, 1999

4. Tanenbaum" Computer Networks " PHI, 1998

5. Sze. S.M, "VLSI Technology "McGraw Hill., 1998

Path													Cost
PATH	1>	3	-	2	-	5	-	9	-	10			: 3065.000000
PATH	2>	3	-	2	-	5	-	12	-	16	-	10	: 3905.781250
PATH	3>	3	-	2	-	6	-	7	-	10			: 2675.000000
PATH	4>	3	-	2	-	6	-	9	-	10			: 2155.000000
PATH	5>	3	-	2	-	7	-	6	-	9	-	10	: 3221.250000
PATH	6>	3	-	2	-	7	-	10					: 2208.750000
PATH	7>	3	-	4	-	1	-	5	-	9	-	10	: 3485.781250
PATH	8>	3	-	4	-	1	-	6	-	7	-	10	: 3235.781250
PATH	9>	3	-	4	-	1	-	6	-	9	-	10	: 2715.781250
PATH	10>	3	-	4	-	1	-	8	-	16	-	10	: 3180.312500
PATH	11>	3	-	4	-	11	-	15	-	7	-	10	: 2531.250000
PATH	12>	3	-	7	-	2	-	5	-	9	-	10	: 4131.250000
PATH	13>	3	-	7	-	2	-	6	-	9	-	10	: 3221.250000
PATH	14>	3	-	7	-	6	-	9	-	10			: 2635.000000
PATH	15>	3	-	7	-	10							: 1622.500000
PATH	16>	3	-	7	-	15	-	17	-	16	-	10	: 3185.781250