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QRS detector circuit

Behzad Ghanavati

Department of Electrical Engineering, Mahshahr Branch, Islamic Azad University, Mahshahr , Iran.

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ABSTRACT

this paper describes a QRS detector system to be implemented using 0.35µm CMOS technology which is used in biomedical applications. The proposed system uses fuzzy logic controller and several analog circuits for detecting QRS complexes and separating these parts from the rest of ECG signal. Simulation results using HSPICE that verify the functionality of system are presented.

Introduction

The electrocardiogram(ECG) is one of the most relatively inexpensive and easily accessible investigational tools for the rapid diagnosis of arrhythmias. A typical waveform from an electrocardiogram (ECG) is shown in fig.1. It consists of several complexes, the P-complex, the QRS-complex, the T-complex and the U-complex.

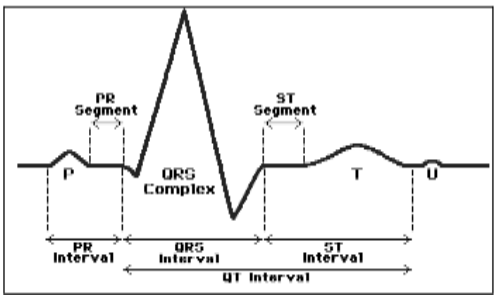

Fig. 1 A typical wave form of an ECG

The dominant component of the ECG is the QRS complex, which indicates the electrical depolarization of the muscles in the ventricle of the heart. [1] Several clinical applications including ECG monitoring system in intensive care unit, operating room and implantable defibrillator require accurate

QRS detection algorithms whiles The QRS is easily recognized by a human observer. Previous automated algorithm detects QRS complexes when the ECG amplitude exceeds a threshold level. [2] Various types of automated algorithms were proposed in the literature for modifying QRS detection. This algorithms use multiple features of the EGG including RR internal, pulse duration and amplitude, to detect QRS complexes. (fig.2)

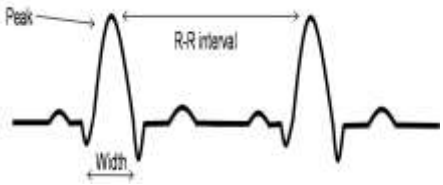

Fig. 2 Features of the ECG

By processing several features, it is less likely that large amplitude but short duration noise would be mistaken for a QRS. Similarly, it is more likely that a true QRS with low amplitude, but normal width and RR internal would be correctly detected.

Fuzzy inference systems are well-suited for this application (fig.3), since detection in this system based on a few amounts of uncertainly which is very similar to the medical reasoning process. Moreover the decision process is extremely easy to understand by human; consequently such easy interpretability allows external changes by experts on the decision process. [3]

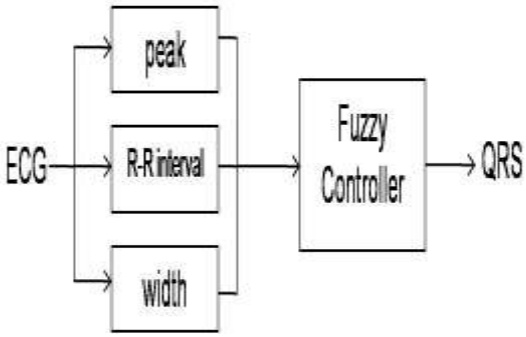

Fig. 3 using fuzzy controller for detecting QRS complexes

In this paper, we have used a fuzzy inference system to identify QRS complexes and designed a new circuit which is used in bio-medical applications. The block diagram of system is presented in section 2 and the method of system for detecting QRS complexes is discussed. Section 3 describes the circuits which are used in this system. Several simulation results are also presented in this section. Conclusion will be presented in section 4.

System description

The proposed chip consists of 2 main parts:

- QRS detector circuit
- Extracting QRS from an ECG circuit

First these parts will be explained separately and then the block diagram of the chip will be presented.

Tele:
E-mail addresses: b.ghanavati@mahshahriau.ac.ir

QRS Detector Circuit

In this system QRS complex will be detected provided that a square wave synchronizes with them, consequently we use a fuzzy controller to adjust this square wave with QRS complexes .R-R internal, pulse duration and amplitude are features of ECG which are measured by specific circuits. The measured features are entered to a controller as inputs parameter. Fuzzy controller evaluates these features and adjusts the output pulse of VCO to be synchronized with QRS complexes. (fig.4)

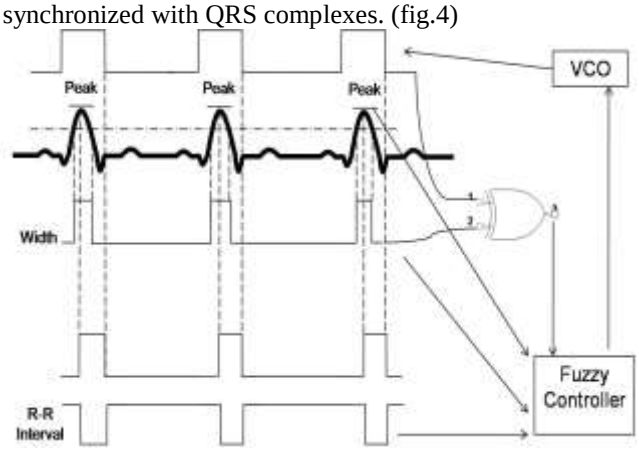

Fig. 4 The proposed QRS detector algorithm

A feedback is used to correct the synchronization process. This feedback is produced by error between the output pulse of VCO and the pulse that shows the width of QRS complex and is done by XOR logical gate. This feedback is also enter to controller and processed by fuzzy controller. Finally, the output of fuzzy controller goes to VCO circuit and makes the output pulse of VCO to be synchronized with QRS complex.

Extracting QRS from an ECG circuit

To separate QRS complexes, we passed ECG signals and synchronize VCO with the same DC voltage level trough an analog median filter. (fig.5) Median Filter pass the median part of the input signals which, in this case, is QRS complexes.

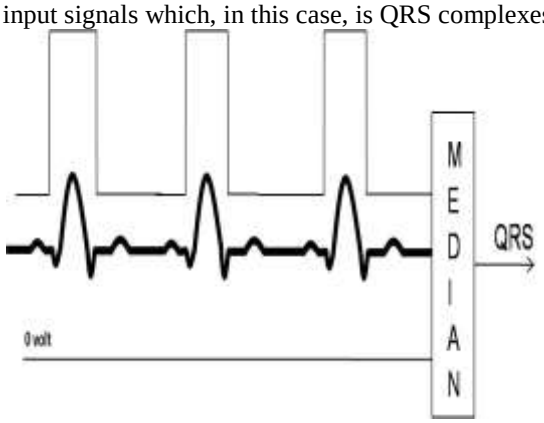

Fig. 5 Extracting QRS from an ECG

The proposed QRS detector chip

The block diagram of proposed system is presented in fig.6

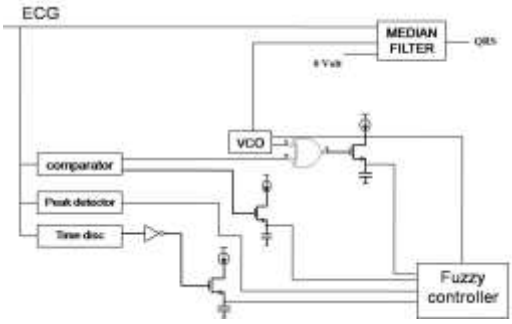

Fig. 6 The proposed QRS detector system

Circuit description

In this section the circuits which are used in the system will be discussed and simulation results of these circuits which verified the functionality of them are presented. Finally, the simulation result for the system will be presented.

Peak detector and time discriminator circuit

Peak detector and time discriminator circuit is used in this work for measuring R-R interval and peak of QRS complexes. Fig.7 shows the Peak detector and time discriminator circuit. [4]

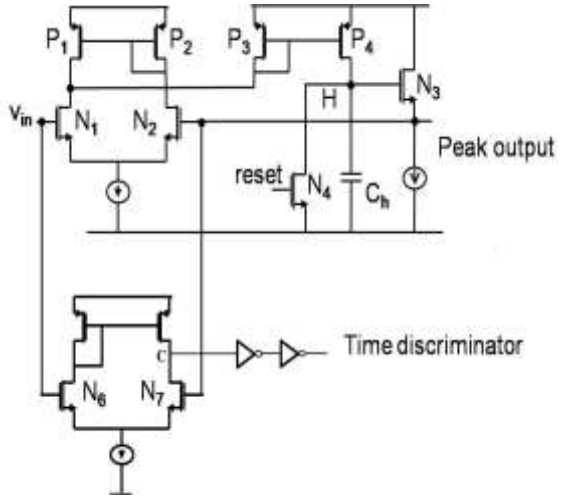

Fig. 7 Peak detector & Time discriminator circuit

An analog positive signal from the shaper, applied at N_1 gate generate a current signal in the P_3-P_4 mirror which is injected in the node H, charging the hold capacitor C_h . The output signal of follower N_3 is fed back to the inverting input of the differential pair (N_2) so the circuit behave a unity gain amplifier. When the peak is reached, the input signal starts to decrease so unbalancing the differential inputs and switching off P_3. The hold capacitance cannot vary its accumulated charge and the peak amplitude value is so acquired.

The peak discriminator generates a trigger after the peak is reached. In facts its input stage (N_6-N_7) compares the shaper and peak-stretcher output and generates a current so setting the node voltage C to about zero. On the leading edge of the shaper signal, the peak-stretcher follows it so maintaining balanced the differential pair N_6-N_7 and setting to zero the current signal in current mirror so the voltage at node C goes high. Two inverters generate the trigger signal with a fast transition.

The time discriminator circuit will be reset by a pulse which is generated by the comparator. The pulse which is used for resetting is started at falling edge of the pulse which is generated by the comparator and shows the width of QRS complexes.

Fig.8 shows the simulation of the proposed circuit

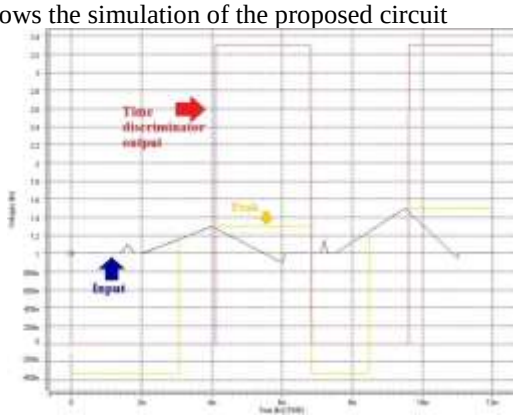

Fig. 8 simulation result of the peak detector and time discriminator circuit

Median filter

An analog median filter is used in this paper [5]. The proposed filter has 3 inputs and one output which almost equal to median part of 3 input voltages.

For implementing analog median filter, transconductance circuit with high gain is used. Fig.9 shows the proposed analog median filter.

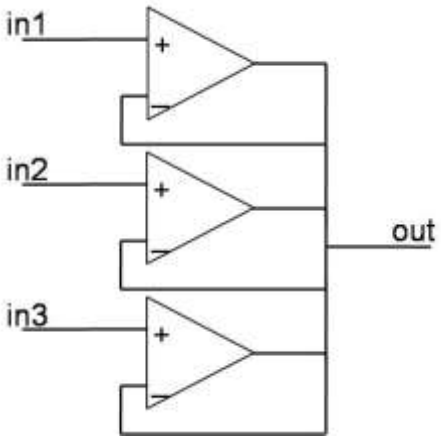

Fig. 9 The proposed analog median filter

In this circuit, the output current of OTA's which input voltage is above the median voltage will saturate in a positive direction, driving a saturation current $I_b/2$ into node out in fig.9 Meanwhile, in the OTA's which input voltage is below the median voltage, the output current will provide a negative output saturation current $I_b/2$ and sink this current from output node.

In this situation, the OTA who has the median voltage is not in saturation mode and can act as a unity gain buffer. So, the output voltage is almost equal to $V_{in,med}$ which is the median voltage among the input voltages.

Fig.10 Shows the transconductance which is used in this filter. Two stage differential pair is used for obtaining higher gain.

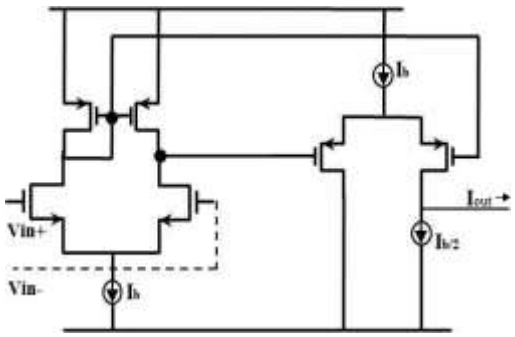

Fig. 10 Two stage differential pair

Since the second stage saturates in current with $I_{out} = \pm I_b/2$ its response to input voltage changes occurs faster than previously reported applications.

Fig.11 shows the simulation result for proposed circuit.

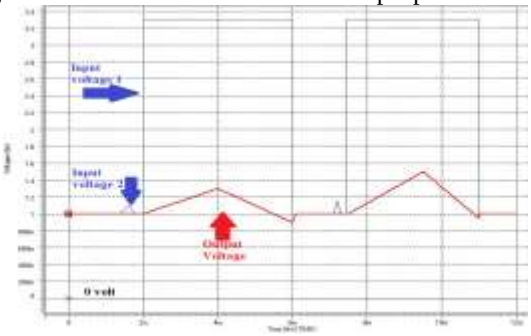

Fig. 11 Simulation result of the median filter

Voltage Controlled oscillator

Pulses which have to synchronize with QRS complexes are generated by the VCO.

The frequencies of QRS complexes are low and between 60 to 250 HZ, so, the VCO which is used have to be suitable for low frequency applications.

The design of a ring oscillator requires to connect odd number of inverters and feedback from the output of the last one to the input of the first one.[6] Since the oscillation frequency is determined by the number of stages and the delay in each stage which is very small for an inverter, typically the achieved frequencies are several hundred MHz to GHz in 0.35 μm CMOS technology. To achieve low frequency output, the number of stages has to be very large which is sometimes unacceptable or increase the delay for each stage instead of increasing the number of stages.

The second choice is used in this work for implementing ring oscillator. So, delay gate is used for implementing ring oscillator instead of using simple inverter gate. Fig.12 shows the propose low frequency VCO.

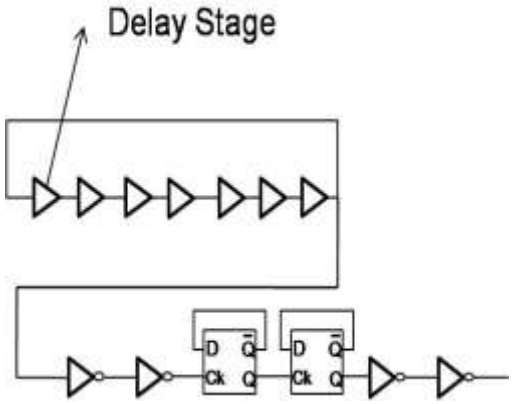

Fig. 12 The low frequency VCO

It is based on a 7-stage of delay cells connected on a loop and followed by a dividing circuit, and a set of inverters that act as the buffer (on a second driving stage) circuit.

In order achieve lower frequency, two dividers by two are used at the output of the loop. It is based on a flip-flop with its inverting output feed back to its input, as shown in Figure 6. The flip-flop turns over each time when the front edge of the input arrives. Hence, it makes the output to be always 50% duty cycle regardless of the frequency. Also, it decreases the oscillating frequency by quarter period. The delay gate is presented in fig.13

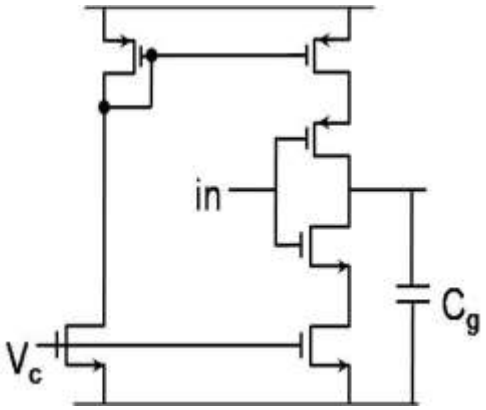

Fig. 13 The delay gate

Fig.14 shows the ability of proposed VCO for generating low frequency

Fig.15 shows the ability of proposed VCO for changing the frequency

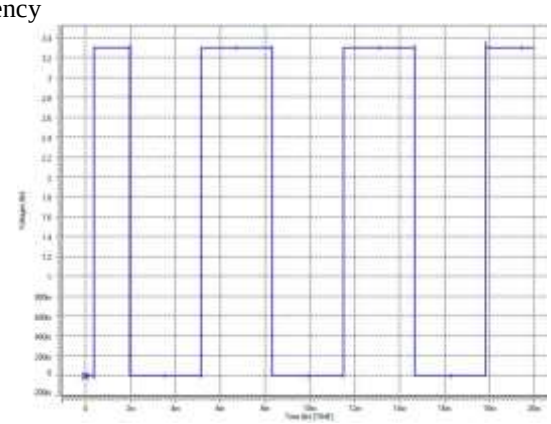

Fig. 14 Simulation result of the VCO (low frequency)

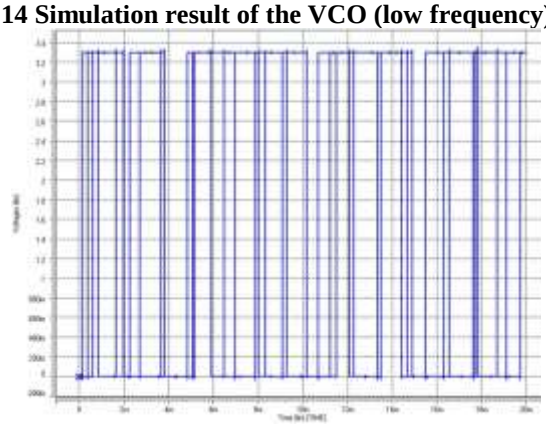

Fig. 15 Simulation result of the VCO (changing the frequency)

Simulation result

Simulation result for the system is shown in fig.16

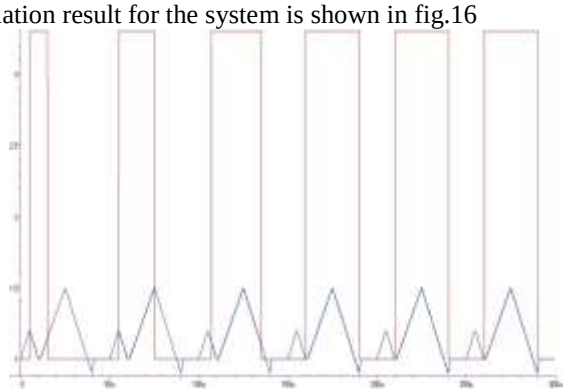

Fig. 16 Simulation result of the system

The VCO pulses are synchronized with QRS complexes by receiving a voltage from fuzzy controller. This synchronization process will be done after at most 5 cycles of ECG.

As mentioned above, if the VCO pulses and ECG are applied to a median filter QRS complexes will separate from the rest of ECG.

Conclusion

In this paper a QRS detector circuit is presented. Since the proposed system uses analog circuits, no need for A/D converter between the ECG and the detector circuit. The system could be used in several biomedical applications.

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Behzad Ghanavati was born in Mahshahr, Iran in 1982.He received his B.Sc degree in Bio medical engineering from Isfahan University, Isfahan, Iran in 2005, and M.Sc degree in Electrical engineering from Urmia University, Urmia, Iran in 2008.His research interests are analog and digital integrated circuit design for fuzzy and neural network application and low voltage analog circuit design. He is currently teacher in Islamic Azad University of Mahshahr (E-mail:b.ghanavati@mahshahriau.ac.ir).