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A review of hybrid multilevel inverter configurations and their comparison

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ABSTRACT

This paper presents the comparison of hybrid multilevel inverters for different voltage and power applications. Hybrid multilevel inverters improve the number of the output voltage level based on a hybrid connection of power cells. Therefore, a given number of levels can be synthesized by several multilevel configurations, significantly increasing flexibility and complexity in the design of hybrid multilevel inverter. The purpose of the circuits presented here is to minimize the reverse voltage stress and the harmonic distortion of the voltage applied to the load. As a characteristic of the proposed cells, some of the switches operate at low frequency while others are switched at high frequency. Different topologies are discussed and reviewed in brief. Voltage sharing and low output-voltage distortion are achieved. This paper presents a survey of different topologies, control strategies and modulation techniques used by these inverters.

Introduction

In various papers the interest is catapulted in multilevel inverters hence introducing different multilevel inverter topologies.

This improves the power quality by inserting small voltage steps in the line to ground voltages. These topologies broadly divided as Neutral Point Clamped (NPC) multilevel inverter, Flying capacitor multilevel inverter and Cascaded multilevel inverter with separated DC sources and within this last classification the hybrid multilevel inverter is included which is further discussed in detail.

The advantages of Hybrid topology are: reduced number of dc sources, high speed capability, low output switching frequency, low switching loss, high conversion efficiency, flexibility to enhance and various topologies for different applications.

Working principle of hybrid multilevel inverters

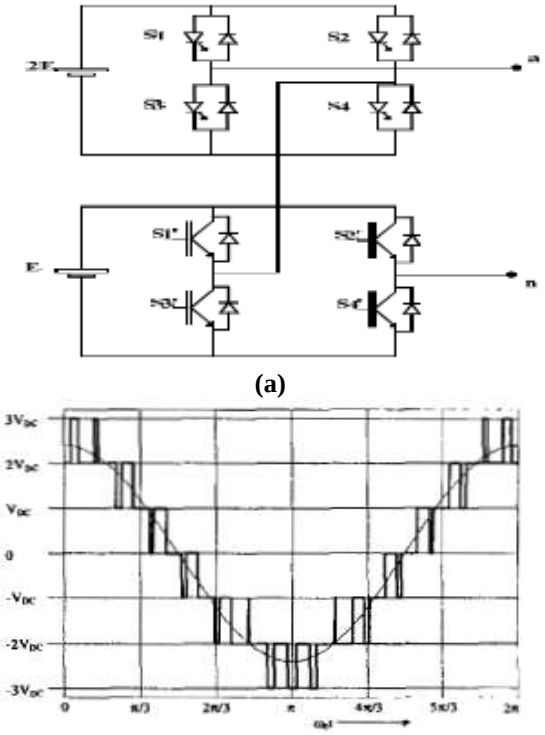
Hybrid multilevel inverter gives multi level operation by using hybrid source, hybrid configuration or hybrid device in such a way to produce output with advantages mentioned above then such topologies are known as hybrid multilevel inverter. Broadly HMLI can be classified as per power circuit configuration and modulation technique used. In this paper discussion is as per power circuit.

Out of many topologies here four topologies are discussed: i) Asymmetrical Hybrid Multilevel Inverter[1] ii) Distinct Series Connected cells Hybrid Multilevel Inverter[2]. iii) Single Phase Hybrid Symmetrical Multilevel Inverter[3] iv) New Hybrid Asymmetrical Multilevel H-bridge Inverter[4],[5].

Various Topologies and Their Comparison

In this section different hybrid multilevel inverter topologies are compared in brief. Fig. 1 (a) shows asymmetrical hybrid multilevel inverter.

This is based on the binary configuration of the voltage sources, meaning that this circuit can synthesize 2^{N+1} -1 levels on the load voltage, N being the number of DC sources.



(a)

(b)

Fig.1 a) Asymmetrical Hybrid Multilevel Inverter. b) Output Voltage

The upper full-bridge is composed by switches of high voltage blocking capability and therefore of low operation frequency (GTO for instance), while the bottom full-bridge is switched at high frequency, but with lower rated voltage (IGBT as an example). Using an appropriate modulation strategy it is possible to synthesize a seven-level voltage waveform: -3E, -2E, -E, 0, E, 2E and 3E. The output voltage wave shape for this circuit is shown in Fig. 1(b).

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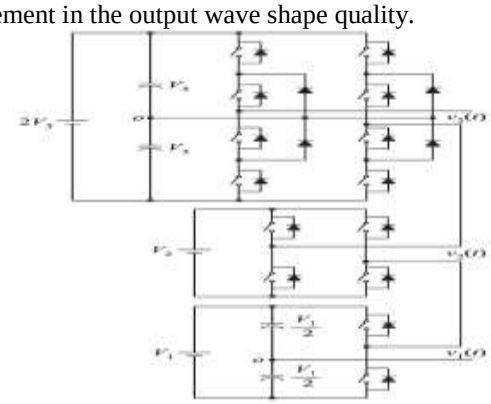
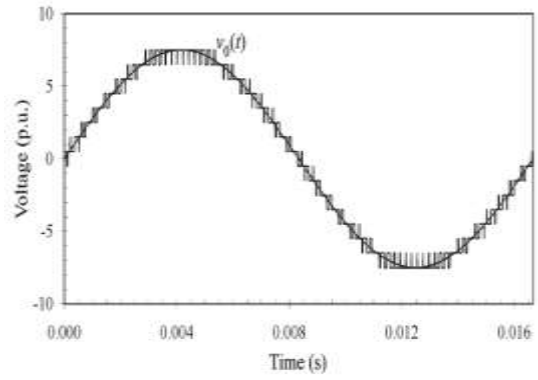
The modulation strategy includes the hybrid modulation concept, which is based on the unique pulse modulation together with the sinusoidal pulse width modulation (PWM). Under this modulation strategy, the slow switches are modulated to commutate at the fundamental frequency, while the fast switches commutate at a higher frequency. As a result of that, there is an improvement in the output wave shape quality.



(a)



(b)

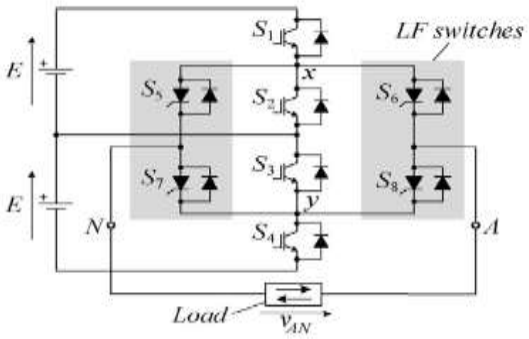
Fig 2. a) Distinct Series Connected cells Hybrid Multilevel Inverter b) Phase voltage.

The spectral response of the output voltage depends on the fast switches, while the whole capacity of voltage generation relies on the slow switches [6].

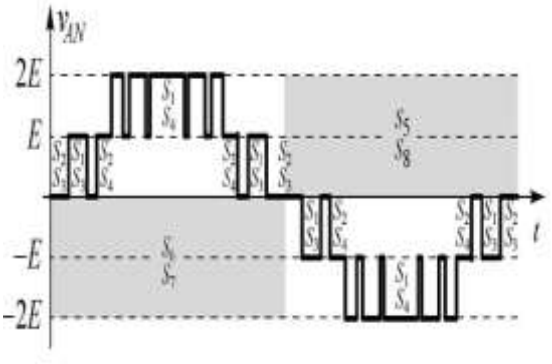
Fig. 2 (a) presents a hybrid multilevel inverter with two-, three- and five-level cells connected in series. The first cell synthesizes two levels with 1-p.u. voltage step, the second cell generates three levels, also with 1-p.u. voltage step, and the third cell synthesizes five levels with 3-p.u. voltage steps. The switching devices of the two-level cell operate at high frequency, while the switches that compose the five-level cell operate at fundamental frequency. This configuration synthesize voltage waveforms with a reduced harmonic content using few series-connected cells and thus output filter size is reduced or even eliminated. The output voltage THD is minimized. Stepped modulation technique is used. The THD of output phase-to neutral voltage obtained with trinary hybrid multilevel inverter (THD = 4.8 %) is smaller than the THD obtained with binary (THD = 7.9 %) and unary hybrid multilevel inverters (THD = 18.3 %) [7].

The circuit of Fig. 3 (a) behaves as a five-level output voltage single-phase inverter. The three level cell switches block voltages of value ´E´, and with proper modulation strategy they operate at high frequency (a few kHz). On the other hand, the H-bridge switches (S5, S6, S7 and S8) must block a higher voltage level of *´2E'*. However, these switches operate only in a semi cycle of the output voltage. Thus, they operate at low frequency commutating at zero voltage. Thus the inverter classified among the hybrid multilevel inverters group. As shown in [8] and [9], the multilevel inverters based on the H-bridge symmetrical cascade have a number of levels in its output voltage given by 2N+1. For Fig.3 b) output voltage levels are also obtained through the same expression [10] and [11].

This topology follows the principle of increasing the number of output waveform voltage levels with less switching devices.

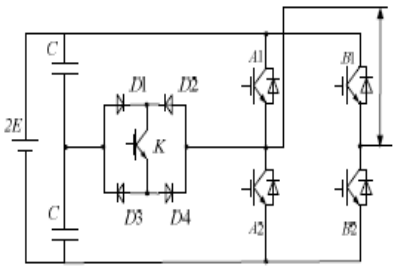


(a)

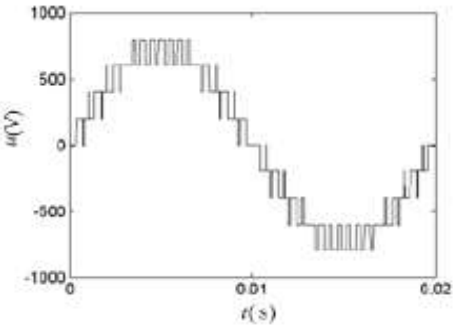


(b)

Fig 3. a) Single Phase Hybrid Symmetrical Multilevel Inverter b) Output Voltage



(a)



(b)

Fig 4. a) A new Hybrid Asymmetrical Multilevel H-bridge Inverter b) Output Phase Voltage

The new Hybrid Asymmetrical Multilevel H-bridge Inverter has an auxiliary bidirectional switch which can output maximum 5-level voltage waveform. In this configuration the two capacitors in the capacitive voltage divider are connected directly across the dc bus, and since all switching combinations are activated in an output cycle, the dynamic voltage balance between the two capacitors is automatically restored.

For asymmetrical multilevel inverters conventional PWM strategies are not suitable because the switching devices of the higher voltage cells would have to operate at high frequency during some time intervals [6], [12] and [13]. Consequently, a hybrid modulation strategy was proposed in [14] and [15], so that higher power cells operate at low frequency and only the lowest power cell operates with high-frequency PWM. A hybrid PWM strategy is used to produce the required output waveforms to reduce the total harmonic distortion of the new hybrid inverter Asymmetrical Multilevel H-bridge Inverter. A novel multi-carrier PD PWM method is used to produce output shown Fig 4 (b). It can be seen that the THD of phase voltage is almost less 5% with the proposed hybrid modulation strategy [4].

Table showing comparison between different hybrid multilevel inverter topologies based on power circuit configuration:

Table I Comparison between different hybrid multilevel inverter topologies

Topology	**Asymmetrical Hybrid Multilevel Inverter**	**Distinct Series Connected cells Hybrid Multilevel Inverter**	**Single Phase Hybrid Symmetrical Multilevel Inverter**	**A new Hybrid Asymmetrical Multilevel H-bridge Inverter**
No. of Devices	Low	High	High	Low
Output levels	2^N +1	2^N +1	2N+1	2(2N)+1
THD	Low	Medium	High	Low
DC Source	N(Unequal)	N(Unequal)	N(Equal)	N(Unequal)
Phase	Single	Single	Single	Single
Modulation Strategy	Hybrid or Programmed Modulation Technique [16]	Hybrid Modulation Technique	Phase Shifted Disposition (PSD)	Phase Disposition (PD) Multi-Carrier PWM

Conclusion

Thus from above discussion it can be concluded that every topology has its own advantages and disadvantages. As asymmetrical multilevel inverters are an alternative to minimizing the harmonic distortion of the output voltages without increasing the number of power devices. The use of different dc voltage values naturally leads to hybrid multilevel topologies, which employ distinct types of semiconductors and modulation strategies, in an effort to optimize the power processing of the overall system. On the other hand, these features increase significantly the flexibility and complexity of hybrid multilevel inverter design.

Distinct Series Connected cells Hybrid Multilevel Inverter reduces the complexity for hybrid topology for distinct applications thus minimizing the number of switching devices and reducing the circulating energy among the series-connected cells.

Compared with an H-bridge cascaded multilevel converter, the number of overall insulated dc sources is reduced in the Single Phase Hybrid Symmetrical Multilevel Inverter while the number of semiconductors is kept the same. Thus, this concept appears as a useful and suitable solution for MV applications where input-side insulation is required along with high efficiency and modularity. Furthermore, by reducing the number of insulated dc supplies, the number of cables connecting the input transformer terminals to the rectifying bridges is reduced.

New Hybrid Asymmetrical Multilevel H-bridge Inverter reduces the harmonic components of output voltage.

Due to the enormous topologies for designing hybrid multilevel inverter, this paper cannot cover all of them, but this paper provides an important basis to define a few hybrid configurations for distinct systems. In future, this paper is extended to discuss other hybrid multilevel inverter topologies, considering additional design specifications, efficiency, and other harmonic distortion factors.

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