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Performance study of variation effect of spacer thickness on Si/$Si_{0.5}Te_{0.5}$-based resonant interband tunneling diode

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ABSTRACT

Si-based resonant interband tunneling diodes (RITD) with spacer thicknesses varying from 2.5 to 25 nm was grown and fabricated at Baghdad University. The effect of spacer thickness on the peak-to-valley current ratio (PVCR), peak current density (J_P), and voltage swing (VS) was studied for determining the static or dynamic read access memory (SRAM, DRAM). By increasing the tunneling spacer thickness up to 12 nm, RITDs with VS are reduced below 0.3V; this is suitable for low-power tunnel diode SRAM applications. The J_P increased as the spacer thickness increased from 2.5nm to 5nm. As the spacer thickness increased above 5nm, the *Jp* decreased. Using a low-current-density in this paper, a bread-boarded one-transistor tunneling-based SRAM (TSRAM) memory cell with low standby power consumption was demonstrated, where the standby power of this 1T TSRAM is estimated to be 65nW/cell using the 10-μm diameter RITDs. The result demonstrates the potential of Si-based tunnel diodes for low-power memory applications.

Introduction

Resonant interband tunneling diodes (RITDs) combine the structures and behaviors of both *intraband* resonant tunneling diodes (RTDs) and conventional *interband* tunneling diodes, in which electronic transitions occur between the energy levels in the quantum wells in the conduction band and that in the valence band [1, 2]. In the beginning a composite SiTe fabricated and deposition on Si-based, i-layer is inserted as tunneling spacer layer between the δ-doped injectors to minimize doping interdiffusion, which leads to a widening of the spacer and a larger tunneling distance [3]. The Low-temperature molecular beam epitaxy (LT-MBE) is used to suppress segregation and diffusion [4, 5], as well as improved speed for logic applications such as multiplexers [6] and analog-to-digital converters [7]. Tunneling diode based SRAM (T-SRAM) uses a tunnel diode pair to store a bit of data, and takes the refresh free and fast write speed of SRAM and puts it into the footprint of a DRAM cell by reducing component count (1 transistor and 2TDs versus 6 transistors in conventional CMOS) [8]. So the integration of tunneling diodes with transistors can increase circuit speed, reduce component count, and reduce power consumption [3], which are all synergistic with the goals of the International Technology Roadmap for Semiconductors (ITRS) [9]. This paper shows the improvement of SiTe (RITDs) device in the memory applications.

Experimental Work

The junction is SiTe/Si deposited by LT-MBE technique. The spacer region appears between two δ-doping layers: the intrinsic Si layer (X δ-doping layer) and $Si_{0.5}Te_{0.5}$ with different thickness (t) (Y δ-doping layer). The RITDs studied here varied the overall spacer thicknesses over the basic Si-based schematic that shown in Fig. (1), where that thicknesses (t) varies from (2.5nm to 25 nm). The Epitaxial growth is achieved with a molecular beam epitaxy (MBE) growth system using elemental Si and Te in electron beam sources. The doping level for both n+ and p+ layers are 5 * 10^{19} cm^{-3}; the X and Y δ-doping sheet concentrations are maintained at 1 * 10^{14} cm^{-2}. Prior to device fabrication, portions of the grown wafers were rapid thermal annealed using a forming gas ambient (N2/H2) in a Modular Process Technology Corporation RTP-600S furnace at various temperatures for 1 min. The wet etchant for mesa etching was $HF:H_2O:HNO_3$ (1:100:100) by volume ratio and etch rates varied between 100 and 150 nm/min.

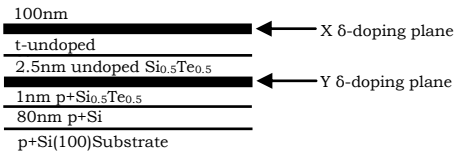

Fig.1 Schematic of the basic Si-based RITD structures with thickness varied from (2.5-25 nm)

Result and Discussion

The relation between PVCR and the spacer thickness explained in Fig. (2). The data for the RITDs with tunneling spacer thicknesses ranging from 12 to 25 nm are plotted together with RITDs with spacer thicknesses ranging from 2.5 to 12 nm from a previous study [10].

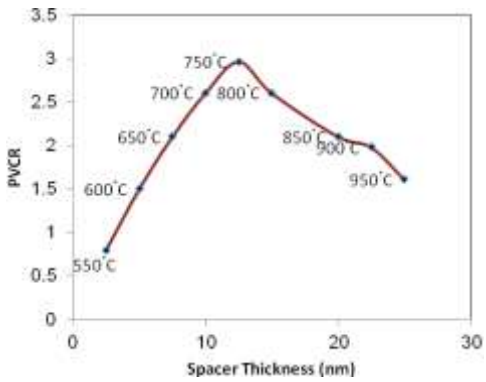

Fig.2 The relation between PVCR and the spacer thickness

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The annealing temperatures that showed in the graph are used to obtain the PVCR. RITD with a 12-nm spacer leads to the highest PVCR. Both decreasing and increasing spacer thicknesses will result in reduced PVCR. It is also observed that the optimal annealing temperature increases from 550 ˚C to 950 ˚C as the spacer thickness increases from 2.5 to 25 nm. The current of an interband tunneling diode consists of three components: quantum mechanical band-to band tunneling through the barrier, the excess current, principally through defects, and the forward-biased thermal diffusion current. The excess current originates from electron tunneling through defects induced within the band-gap states. Chynoweth *et al.* [11] derived the excess current equation as:

$$I_x = A \times D_x \exp\left\{\left(\frac{-a_x \times W \times e^{0.5}}{2}\right) \times \left[E_g - eV + 0.6e\left(V_n + V_p\right)\right]\right\} \quad (1)$$

where A is a voltage- and temperature-independent pre-factor, D_x is the density of states in the band gap at a corresponding energy related to the forward bias V , α_x is a material constant containing a reduced effective mass, W is the tunneling barrier width, Eg is the band gap, e is the electron charge, V_n is the potential difference (in volts) between the Fermi level on the n-type side and the bottom of the conduction band, and V_p is the potential difference (in volts) between the Fermi level on the p-type side and the top of the valence band.

Since the PVCR drops as the spacer thickness increases from 12 to 25 nm (Fig. 2), it is hypothesized that the desired band-to-band tunneling current decays faster than the excess current with increasing tunneling barrier width. In other words, the tunneling selection rules are reduced for larger spacer thicknesses. The hypothesized tunneling selection rule can be validated by the fact that RITDs with thin spacers outperform RITDs with thick spacers under the same low-temperature annealing conditions [12]. This fact indicates that a thin tunneling barrier intrinsically allows more desirable band-to-band tunneling current than excess current; therefore, a larger PVCR ensues. In essence, the characteristic length scale for the desired band-to-band tunneling is approximately the thickness of the tunneling barrier, whereas defect related tunneling passes through at least one intermediary defect site within the tunneling barrier, so its effective length scale will be less.

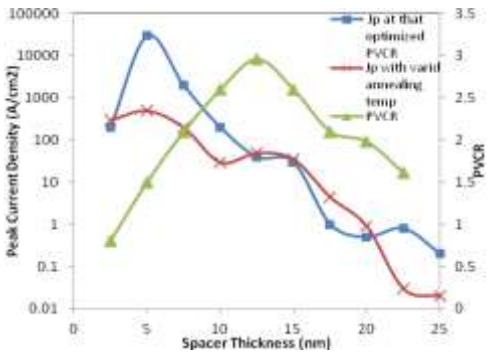

Fig.3. The effect of spacer thickness on PCDs and PVCR.

When the spacer thickness is reduced from 12 to 2.5 nm the PVCR decreases along with a lowering of the optimal annealing temperature, which seems to be in conflict with the hypothesized tunneling selection rules aforementioned. However, as the spacer thickness decreases for very narrow spacers, another phenomenon occurs. An increasing number of opposite carrier-type dopant pairs [11] are able to be formed within the tunneling barrier due to the close proximity of the X and Y delta-doping layers (Fig.1), which partially interdiffusion with each other, and this is exacerbated as the tunneling spacer is reduced toward 1 nm. These dopant pairs can introduce energy states within the band gap [13, 14]; therefore RITDs with thin tunneling spacers, point defects formed during LT-MBE cannot be effectively removed because the annealing temperature has to be kept low enough so that minimal interdiffusion occurs and fewer dopant pairs are formed during the annealing process.

RITDs with thick spacers have less point defects and dopant pairs than RITDs with thin spacers, which imply more excess current and smaller PVCR. By using Si/SiTe RITD design in this paper at 12 nm, there's an optimal spacer thickness for the highest PVCR depending on two mechanisms: quantum mechanical and excess current. In Fig.3 the character (*x*) indicates the maximum PVCR that can be obtained by varying the annealing temperature for each RITD spacer thickness. The character (■) shows the corresponding *Peak Current Density* (PCD) at that optimized PVCR. The character (▲) illustrates the spread in *PCD* at various temperatures as the annealing temperature is varied; the Figure above shows that PCD was increased with spacer thicknesses decreasing. Fig.4 shows the voltage-current (V-I) characteristics of 550 ˚C annealing RITD with spacer thickness varied from 12 to 25 nm which shows that negative differential resistance become more expand with spacer thickness increase. Fig.5 illustrates the relation between J_P and PVCR in a linear relation. As shown in Fig.6 the voltage (VS) plotted as relation with PVCR where the character (▲) illustrates VS with the range of thickness from 2.5 to 12 (nm) and the character (■) show VS at range from 12 to 25 (nm). Fig.7 shows the signals of a 100-kHz word line and a 50-kHz bit line as well as the resulting waveform measured at the SNR, clearly demonstrating the first Si-based tunneling-based SRAM (TSRAM) circuit. In the WRITE operation, when the word line is high, the SNR will copy the value from the bit line and keep latched until the next WRITE cycle begins. The states of 0 and 1 are 0.05 and 0.46 V, respectively. The standby power of this 1T TSRAM is estimated to be 65nW/cell using the 10-μm diameter RITDs.

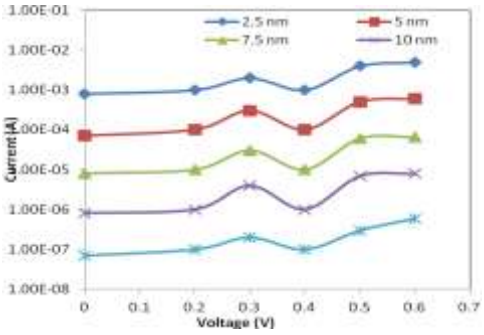

Fig.4. Current and Voltage characteristics of RITDs

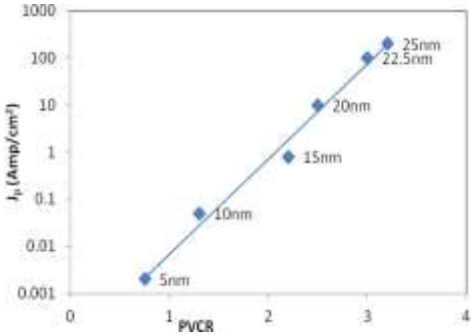

Fig.5. Function of J_p with PVCR

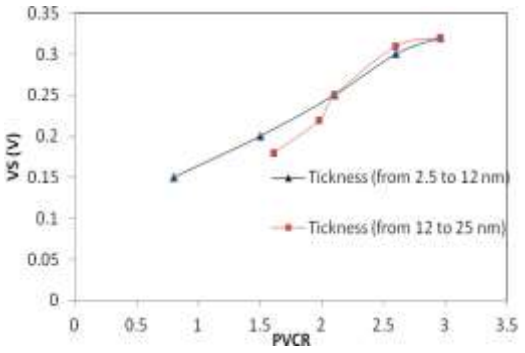

Fig.6. VS plotted with PVCR

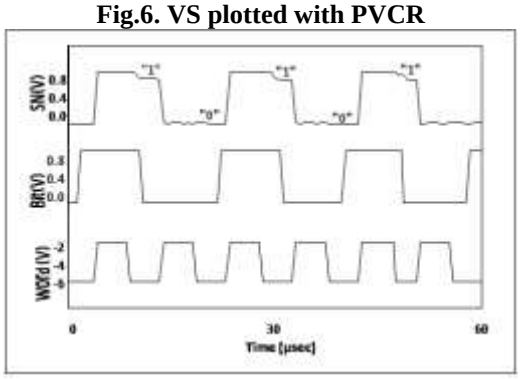

Fig.7. Oscilloscope image of the measured waveforms from the word line, Bit line, and the resulting SN, showing the 1T TSRAM WRITE functionality

Conclusion

In this paper, the Si-based RITDs grown by LT-MBE and PVCR, J_P and VS are depend on the varying of spacer thickness of Si/SiTe, where the maximum PVCR was found at 12 nm of spacer thickness. The J_P was increased as the spacer thickness increased from (2.5-5) nm, then it sharply decreased after 5nm. The standby power of 1T TSRAM was estimated to be 65nW/cell using the 10-μm diameter of RITDs. The highest voltage source was at 12nm. The characteristics of Si/SiTe are suitable for low-power memory applications.

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