Available online at www.elixirpublishers.com (Elixir International Journal)

Advanced Engineering Informatics

Elixir Adv. Engg. Engg. 52A (2012) 11658-11661

ISSN: 2229-712X

Implementation of energy efficient adder for ALU using modified pass transistor logic

E. Suresh and S.Jeyam Jacqueline

Department of IT, The Kavery Engineering College, Mecheri.

ARTICLE INFO

Article history:

Received: 21 March 2012;

Received in revised form:

19 November 2012;

Accepted: 23 November 2012;

Keywords

Arithmetic,

Full-adder,

High-speed,

Low-power.

ABSTRACT

We present two high speed and low power full adder cells designed with modified pass transistor logic styles that lead to have a reduced power delay product (PDP) as compared to the previous logics DPL and SR-CPL logic. We carried out a comparison against other full adders reported as having a low PDP, in terms of speed and power consumption. All the full-adders were designed with a 0.12µm CMOS technology. Simulations of the circuit show that the proposed full-adders have reduced the power from 0.326mW to 0.242mW.

Introduction

Energy efficiency is one of the most required features for modern electronic systems designed for high-performance and/or portable applications. In one hand, the ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. On the other hand, the general trend of increasing operating frequencies and circuit complexity, in order to cope with the throughput needed in modern high-performance processing applications, requires the design of very high-speed circuits. The power-delay product (PDP) metric relates the amount of energy spent during the realization of a determined task, and stands as the more fair performance metric when comparing optimizations of a module designed and tested using different technologies, operating frequencies, and scenarios.

Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application-specific digital signal processing (DSP) architectures and microprocessors. This module is the core of many arithmetic operations such as addition/subtraction, multiplication, division and address generation. As stated above, the PDP exhibited by the full-adder would affect the system's overall performance. Thus, taking this fact into consideration, the design of a full-adder having low-power consumption and low propagation delay results of great interest for the implementation of modern digital systems.

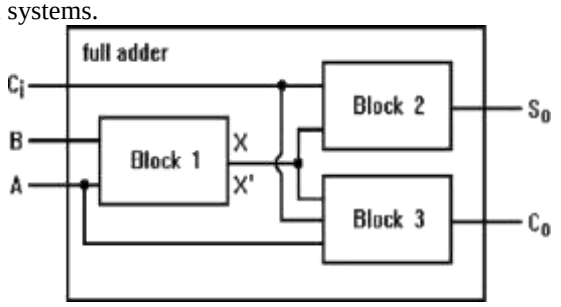

Fig. 1. Full-adder cell formed by three main logical blocks

In this paper, we report the design and performance comparison of two full-adder cells implemented with an alternative internal logic structure, based on the multiplexing of the Boolean functions XOR/XNOR and AND/OR, to obtain balanced delays in SUM and CARRY outputs, respectively, and pass-transistor powerless/groundless logic styles, in order to reduce power consumption. The resultant full-adders show to be more efficient on regards of power consumption and delay when compared with other ones reported previously as good candidates to build low-power arithmetic modules.

This paper is organized as follows. Section II presents the internal logic structure adopted as standard in previous papers for designing a full-adder cell. Section III introduces the alternative internal logic structure and the pass-transistor powerless/groundless logic styles used to build the two proposed full-adders. Section IV explains the features of the simulation environment used for the comparison carried out to obtain the power and speed performance of the full-adders. Section V reviews the results obtained from the simulations, and Section VI concludes this work.

Ii. Previous full-adder optimizations

Many papers have been published regarding the optimization of low-power full-adders, trying different options for the logic style (standard CMOS), differential cascade voltage switch (DCVS), complementary pass-transistor logic (CPL), double pass-transistor logic (DPL), swing restored CPL (SR-CPL), and hybrid styles, and the logic structure used to build the adder module.

The internal logic structure shown in Fig. 1 has been adopted as the standard configuration in most of the enhancements developed for the 1-bit full-adder module. In this configuration, the adder module is formed by three main logical blocks: a XOR-XNOR gate to obtain (Block 1), and XOR blocks or multiplexers to obtain the SUM (*So*) and CARRY (*Co*) outputs (Blocks 2 and 3).

Tele:

E-mail addresses: s.jeyam1989@gmail.com

A deep comparative study to determine the best implementation for Block 1 and an important conclusion was pointed out in that work: the major problem regarding the propagation delay for a full-adder built with the logic structure shown in Fig. 1, is that it is necessary to obtain an intermediate signal and its complement, which are then used to drive other blocks to generate the final outputs.

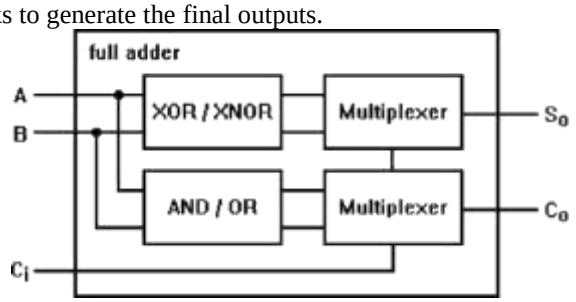

Fig. 2. Alternative logic scheme for designing full-adder cells

Thus, the overall propagation delay and, in most of the cases, the power consumption of the full-adder depend on the delay and voltage swing of the signal and its complement generated within the cell. So, to increase the operational speed of the full-adder, it is necessary to develop a new logic structure that does not require the generation of intermediate signals to control the selection or transmission of other signals located on the critical path.

Table I
True-Table For A 1-Bit Full-Adder: A, B, And C Are Inputs; So And Co Are Outputs

C	B	A	So	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Iii. Alternative logic structure for a full-adder

Examining the full-adder's true-table in Table I, it can be seen that the *So* output is equal to the A XOR B when C=0 and it is equal to A XNOR B when C=1. Thus, a multiplexer can be used to obtain the respective value taking the input C as the selection signal. Following the same criteria, the *Co* output is equal to the A+B value when C=0 and it is equal to A . B value when C=1. Again, C can be used to select the respective value for the required condition, driving a multiplexer. Hence, an alternative logic scheme to design a full-adder cell can be formed by a logic block to obtain the signals A XOR B and A XNOR B, another block to obtain the A . B and A+B signals, and two multiplexers being driven by the input to generate the *So* and *Co* outputs, as shown in Fig. 2.

Proposed logic:

The proposed XOR and XNOR circuits are based on the modified version of a CMOS inverter and pass transistor logic. In proposed circuit-I, for XOR when the input B is at logic 1, the inverter circuit functions like a normal CMOS inverter. Therefore, the output is the complement of input A. When the input B is at logic 0, the CMOS inverter output is at high impedance. However, the PMOS pass transistor is ON and the output gets the same logic value as input A. The operation of the whole circuit is thus like a 2-input XOR circuit. However, it performs non full-swing operations for some input patterns causing their corresponding outputs to be degraded by |Vth|. The proposed XOR-XNOR circuit-I is shown in Fig. 5

The features and advantages of this logic structure are as follows.

• The no of PMOS and NMOS transistors in CMOS are reduced in modified pass transistor logic as compared to the previous DPL and SR-CPL logic

• There are not signals generated internally that control the selection of the output multiplexers. Instead, the

• input signal, exhibiting a full voltage swing and no extra delay, is used to drive the multiplexers, reducing so the overall propagation delays.

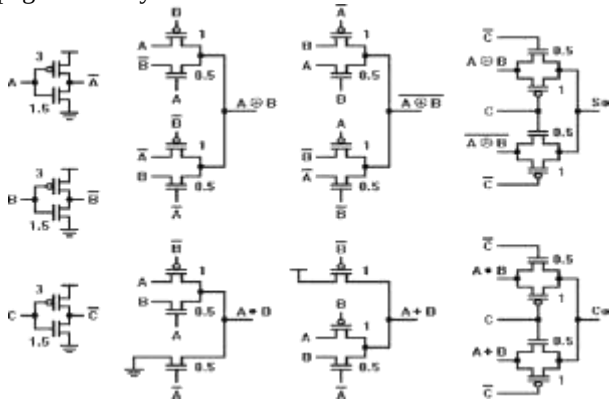

Fig. 3. Full-adder designed with the proposed logic structure and a DPL logic style .

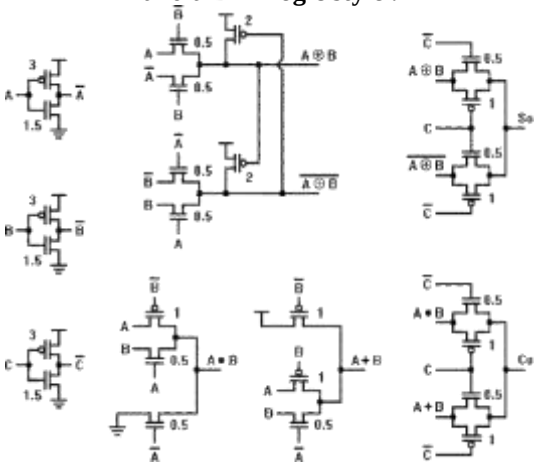

Fig. 4. Full-adder designed with the proposed logic structure and a SR-CPL logic style .

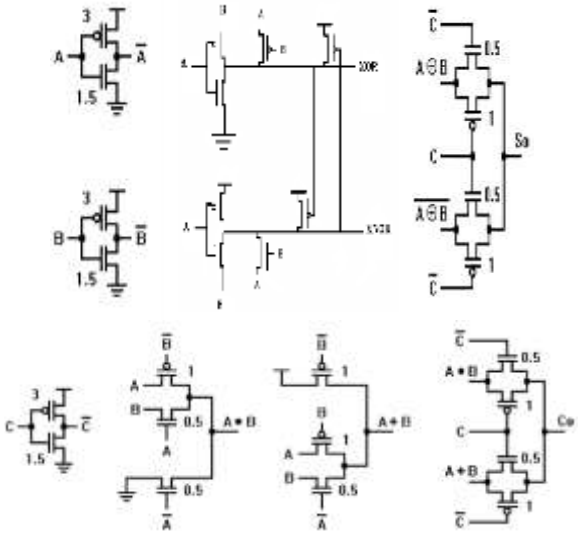

Fig. 5. Full-adder designed with the proposed logic structure and a modified pass transistor logic style (Ours1).

• The capacitive load for the input has been reduced, as it is connected only to some transistor gates and no longer to some drain or source terminals, where the diffusion capacitance is

becoming very large for sub-micrometer technologies. Thus, the overall delay for larger modules where the signal falls on the critical path can be reduced.

- The propagation delay for the *So* and *Co* outputs can be tuned up individually by adjusting the XOR/XNOR and the AND/OR gates; this feature is advantageous for applications where the skew between arriving signals is critical for a proper operation (e.g., wave-pipelining), and for having well balanced propagation delays at the outputs to reduce the chance of glitches in cascaded applications.
- The inclusion of buffers at the full-adder outputs can be implemented by interchanging the XOR/XNOR signals, and the AND/OR gates to NAND/NOR gates at the input of the multiplexers, improving in this way the performance for load-sensitive applications

Two new full-adders have been designed using the logic styles DPL and SR-CPL, and the new logic structure presented in Fig. 5. Fig. 3 presents a full-adder designed using a DPL logic style to build the XOR/XNOR gates, and a pass-transistor based multiplexer to obtain the *So* output. In Fig. 4, the SR-CPL logic style was used to build these XOR/XNOR gates. In both cases, the AND/OR gates have been built using a powerless and groundless pass-transistor configuration, respectively, and a pass-transistor based multiplexer to get the *Co* output.

Simulation Environment

The simulation environment has been used for comparing the full-adders The main advantage of using this simulation environment is that the following power components are taken into account, in addition to the dynamic one. Simulation can be by using the softwares Microwind Layout Editor and DSCH schematic.

Simulation Results

We compared the performance of 3 full-adders, named: DPL, SR-CPL and Ours1. The schematics and layouts were designed using a TSMC 0.18-µm CMOS technology, and simulated using the Microwind layout editor and DSL schematic to determine the power consumption features of the designed full-adders, and also to measure the propagation delay for the output signals. In order to have a fair comparison, we took the transistors sizes for each full-adder that were reported in the correspondent paper, and made all the layouts with a homogeneous arrangement.

Scheme	Power	Delay	Maximum Current Idd(max)
DPL Logic	0.289mW –	0.556ns at 1.8G 1.664ns at 0.61G	2.399mA
SR-CPL Logic	0.326mW	0.550ns at 1.82G 0.816ns at 1.23G	3.006mA
Modified Pass Transistor Logic	0.242mW	0.556ns at 1.8G 1.664ns at .61G	1.806mA

Table II shows the simulation results for full-adders performance comparison, regarding power consumption, propagation delay, and Maximum current. All the full-adders were supplied with 1.8 V. This table reports the power consumption, Propagation delay and maximum current drawn.

From the results in Table II, we can state the following.

- The proposed logic has reduced the power consumption. For DPL logic the power consumption is 0.289mW whereas for SR-CPL Logic it is 0.326mW. The modified pass transistor Logic (Proposed Logic) has consumed less power 0.242mW
- As Shown in the table II, the maximum current drawn for the proposed logic was reduced to 1.806mA as compared to the DPL and SR-CPL Logic. For DPL logic, the current drawn is 2.399 mA and For SR-CPL Logic, the current drawn is 3.006 mA.
- The propagation delay for all the three full adder cells is almost same.

Conclusion

An alternative internal logic structure for designing full-adder cells was introduced. In order to demonstrate its advantages, two full-adders were built in combination with pass transistor powerless/groundless logic styles. They were designed with a 0.18 µm CMOS technology, and were simulated and compared against other energy-efficient full-adders reported recently.

Microwind Layout editor and DSCH schematic simulations showed power consumption is reduced to 0.242mW from 0.289mW and 0.326mW.

References

[1] A. M. Shams and M. Bayoumi, "Performance evaluation of 1-bit CMOS adder cells," in *Proc. IEEE ISCAS*, Orlando, FL, May 1999, vol. 1, pp. 27–30.

[2] N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design, A System Perspective*. Reading, MA: Addison-Wesley, 1988, ch. 5.

[3] K. M. Chu and D. Pulfrey, "A comparison of CMOS circuit techniques: Differential cascode voltage switch logic versus conventional logic," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 4, pp. 528–532, Aug. 1987.

[4] K. Yano, K. Yano, T. Yamanaka, T. Nishida, M. Saito, K. Shimohi-gashi, and A. Shimizu, "A 3.8 ns CMOS 16 2 16-b multiplier using complementary pass-transistor logic," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 388–395, Apr. 1990.

[5] M. Suzuki, M. Suzuki, N. Ohkubo, T. Shinbo, T. Yamanaka, A. Shimizu, K. Sasaki, and Y. Nakagome, "A 1.5 ns 32-b CMOS ALU in double pass-transistor logic," *IEEE J. Solid-State Circuits*, vol. 28, no. 11, pp. 1145–1150, Nov. 1993.

[6] R. Zimmerman and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.

[7] M. Zhang, J. Gu, and C. H. Chang, "A novel hybrid pass logic with static CMOS output drive full-adder cell," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2003, pp. 317–320.

[8] C. Chang, J. Gu, and M. Zhang, "A review of 0.18- m full adder perfor-mances for tree structured arithmetic circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 6, pp. 686–695, Jun. 2005.

[9] S. Goel, A. Kumar, and M. Bayoumi, "Design of robust, energy-effi-cient full adders for deep-submicrometer design using hybrid-CMOS logic style," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 12, pp. 1309–1320, Dec. 2006.

[10] S. Agarwal, V. K. Pavankumar, and R. Yokesh, "Energy-efficient high performance circuits for arithmetic units," in *Proc. 2nd Int. Conf. VLSI Des.*, Jan. 2008, pp. 371–376.

[11] D. Patel, P. G. Parate, P. S. Patil, and S. Subbaraman, "ASIC imple-mentation of 1-bit full adder," in *Proc. 1st Int. Conf. Emerging Trends Eng. Technol.*, Jul. 2008, pp. 463–467.

[12] N. Zhuang and H. Wu, "A new design of the CMOS full adder," *IEEE J. Solid-State Circuits*, vol. 27, no. 5, pp. 840–844, May 1992.
[13] M. Aguirre and M. Linares, "An alternative logic approach to imple-ment high-speed low-power full adder cells," in *Proc. SBCCI*, Floria-nopolis, Brazil, Sep. 2005, pp. 166–171.
[14] A. M. Shams, T. K. Darwish, and M. Bayoumi, "Performance analysis of low-power1-bit CMOS full adder cells," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 10, no. 1, pp. 20–29, Feb. 2002.
[15] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," *IEE Proc. Circuits Devices Syst.*, vol. 148, no. 1, pp. 19–24, Feb. 2001.
[16] Synopsys, San Jose, CA, "Nanosim user guide," A-2008.03, Mar. 2008.
[17] Synopsys, San Jose, CA, "HSPICE user guide," A-2007.12, Dec. 2007.