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Application specific NOC: power optimization by custom topology generation using network partitioning approach

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ABSTRACT

In Networks-On-Chips, (NOC) global interconnection links and routers are the main sources of the power Consumption. In Application Specific NOC (ASNOC) power can be minimized by mapping the Processing Element (PE) on the custom topology rather than mapping on the standard topologies. In ASNOC, the design of the topology plays an important role in minimizing the power consumption. In this paper, we propose a custom topology generation algorithm using network partitioning, to reduce the power of the global interconnection links that connects the router to router. The proposed method is validated through a case study for benchmark video applications MPEG 4 decoder and PIP. The experimental case study shows 26.8% and 37.5% of power saving for the applications MPEG 4 decoder and PIP respectively compared to the existing algorithm. We also achieve 11.76% and 9 % of reduction in average number of hops for MPEG 4 decoder and PIP respectively.

Introduction

As the technology scales down, the number of processors, memory, and the accelerator cores on the System on chip (SOC) increase rapidly. This results in increased communication and computation complexity. In SOC, the bus based communication limits the performance and increases the energy consumption due to the increased communication complexity. So, today's SOC requires new on-chip interconnects that are energy efficient and have high performance [1]. Networks-On-Chip (NOC) has emerged as a viable solution for designing energy efficient and high performance architectures, for Multi Processor SOC (MPSOC) [2]. In NOCs, instead of the bus based communication system, micro networks are used to interconnect various IP cores [1]. In NOC, the area and the power overhead must be minimized. The uses of the standard topologies like Mesh, Torus, Star, Binary Tree and Ring for the design of micro network in NOC results in poor performance and have a larger power and area when used for SOC [1]. This necessitates the design of Application Specific Topology that minimizes the power consumption. One of the most effective approaches to address the power consumption of Application Specific NOC is to select the network topology that achieves lowest power consumption [3]. In this paper, the power consumption of the NOC router for different number of ports and the power consumption of the global interconnection links at circuit and system levels of abstractions are analyzed. Based on this analysis, we propose a graph theory based novel partitioning algorithm to partition the Communication Task Graph (CTG) into three. We map each partition on standard topologies and select one topology for each partition that has low power. Then we connect the selected topology from each partition to form a custom Hybrid topology. The proposed partitioning algorithm is validated through a case study for benchmark video applications MPEG 4 decoder and PIP.

This paper is organized as follows: In section 2, overview of the related work is presented. In section 3, we present graph theoretical approach for the design of topological structure for NOCs. In section4, we present the power analysis of the global interconnection links and the routers of NOC. The proposed methodology for power optimization is presented in section 5. In section 6, we present the evaluation of the proposed methodology and finally in section 7, we present the conclusions and future work.

Related work

Power optimization for Application Specific NOC has been presented by many researchers. Floor plan [1] information is used for designing Application Specific NOC (ASNOC) topology and better power reduction is achieved for the custom topology than standard topologies. In [4]- [7] the applications have been mapped on the standard topologies and the performance is evaluated to select the optimum topology. Low power custom topology has been designed in [8]- [10] using algorithm and evaluated the performance of the algorithm for benchmark video applications. Network partitioning approach is carried out [11] to partition the CTG and the each partition is mapped onto only one type of the topology. Long range insertion [12] is used on the top of the regular topologies to select the Application Specific topology for the greatest performance. Power optimization through network partitioning and long range insertion [13] is considered and the topology is partitioned into 2 and each partition is mapped on 11 standard topologies to select the topology that consumes low power using an exhaustive search method. In [14], automatic energy model for NOC Processing Element is presented and this model is used to analyze the power consumption of NOC at the early stage. Energy model for all the NOC components and interconnection links are presented in [15]. Dynamic power consumption the NOC switch fabric at the bit level is presented in [16]. In [17] the author developed an analytical model for the

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global interconnection link. A tool named OIDIPUS (On-Chip Interconnect Design Interface for Point to Point Unidirectional Signaling) [20] is developed for partitioning a given network and the results were compared with human designed partitioning. Two heuristics algorithms namely CLUSTER and DECOMPOSE [21] are presented to systematically examine different set partitions of the communication flows and Rectilinear- Steiner-Tree based algorithm is proposed for generating an efficient network topology for each group in the partition. In [22], the concept of voltage- frequency island (VFI) is used for achieving fine grain system level power management in networks-on -chip communication. Here, the NOC architecture is divided into multiple VFIs, supply and the threshold voltages is assigned to each VFI.

Graph Theoretical Approach for the design of network on chip topology

In this section, we analyze the graph theoretical concept in designing low power custom topology by partitioning the graph. The topology of any interconnection network can be represented by a graph. A graph G=(V, E) is defined as a set of vertices, V, and a set of edges, E and each node $v_i \in V$ represents a core or processing element (PE) and a edge $e_{ij} \in E$ is an edge that connects vertices 'v' pair-wise and is undirected. The communication between two cores or PEs is represented as the number of data packets transmitted between two cores per time period. Each edge e_{ij} is represented by a weight factor λ_{ij} that denotes average number of packets transmitted between two cores v_i, v_j.. This graph is represented as a Communication Task Graph (CTG). The following figure 1(a) shows the example CTG and figure 1(b) shows its corresponding Communication Distribution matrix (CDM) λ matrix.

In this paper, we analyze the power consumption of the interconnection link by considering the following assumption as discussed by Elmiligi [13].

- Any given application can be represented as a Communication Task Graph (CTG).
- Fixed bus width is considered for all the interconnection links that connect router to router.
- Network Interface is inbuilt in the core.
- Same length is assumed for the link that connects router-to- core.
- Shortest path routing is used.

Based on this assumption, the power consumption of the router-to-router interconnection link depends on

(i) The number of packets transmitted per time period between sources PE to destination PE.

(ii) The number of hops the packets takes to reach the destination.

4 Power Analysis of the global interconnection link and the router. In NOC, data are sent through links (bunch of wires) from one PE to another via intermediate routers. Here, the power consumed is the sum of the power consumed by the links (through the wires), nodes (processing elements (PE)) and intermediate routers which in turn include the power consumed by internal components such as buffers, arbiters and crossbars during switching action. The power consumption of the PE is fixed and it does not depend on the topological structure of NOC. Hence, in this section, we analyze the power consumption of the router and the global interconnection link.

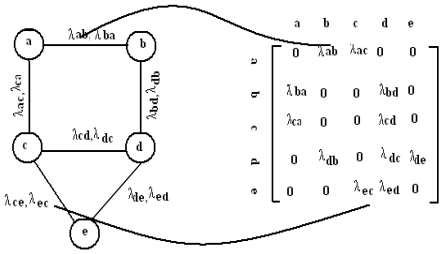


Figure 1 (a) Communication task graph

Figure 1 (b) Communication Distribution matrix

Power Analysis of NOC router.

In NOC router, the power is dissipated on three components: (i). Internal node Switches (ii). Internal buffers used to store the flits temporarily.(iii) The interconnect wire inside the switch [16]. The power consumed on these components change under different traffic conditions. The design of the network on chip router consists of four parts. (i). The input port (ii) The arbitration unit (iii) The crossbar switch (iv) The output port. The input port has buffers to store the incoming data and header decoder unit decodes the destination address. We use input queuing for buffer placement and the round robin algorithm for arbitration. Multiplexer and De multiplexer are used as crossbar switch. The output port has only two flits buffer. The basic router unit is shown in the figure 2. This router has five ports. When the flits arrive at the input port, the flits are stored in the buffer and the header unit decodes the destination address from the header flit. It sends the request to the output port. The arbiter presents in the output port gives access to the input port in round robin fashion, if more than one input ports request the same output port. The input port that receives the access sends the flits through crossbar switch to the output port. We take 128 bits of packet (32 flits each of 8 bit width). The input buffer size is 8 flit buffers and wormhole switching is used. We analyze the area and the power consumption of NOC router by designing the five port router in Verilog HDL and implemented using 0.18µm technology from TSMC using Cadence Encounter RTL compiler [23]. Then we modified the router architecture by changing the no of ports in the routers as 2,3,4,5,7,12 based on the requirement of the topology and analyze the area and the power consumption for all the router architectures. The results of the area and power consumption for different number of ports are shown in figure 3.

4.2 Power Analysis of global Interconnection links We Analyze the power consumption of global interconnection links at two levels of abstractions as discussed by Elmiligi [13].

(i) System level of abstraction.

(ii) Circuit level of abstraction.

System level of abstraction

Assuming the shortest path routing, and one unit of power is consumed when a packet is transmitted over a unit length, the power consumption of the global interconnection link is measured at system level of abstraction by calculating how many

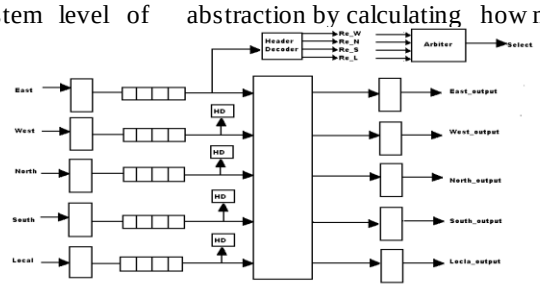


Figure 2. Five port input queuing router architecture

Power units are consumed to transmit all the data packets given in the CTG. To calculate the total power units consumed to transmit all the data packets a unique connectivity matrix is

formed using graph theory concept. The connectivity matrix ($B_{i\ j}$) represents the minimum number of hops a packet travels during its transmission from source PE to destination PE. We assume equal length for all the links for a given topology. The connectivity matrix B= | $B_{i\ j}$| for a mesh topology is shown in figure 4.

The total power consumed in the global interconnection links at the system level of abstraction can be estimated as in [13]

$$Psys = \sum_{i=1}^{n} \sum_{j=1}^{n} \lambda ij\, Bij.Up \quad (1)$$

Where i and j are source and destination PE indexes respectively. λij is the average number of packets transmitted per time unit from source PE i to destination PE j. B_{ij} is the minimum number of hops a packet travels from source PE to destination PE. U_p is the unit power.

Circuit level of abstraction

At the circuit level the total power consumed in global interconnection links can be approximated as discussed in by Kim [17]. Optimal repeaters may be inserted in each wire in a cascaded structure to model the delay of the wire [17] as shown in figure 5.

The average power consumed in the global interconnect can be approximated by

$$P_{link} = \frac{1}{2}(Cw + Crep)V_{dd}^2 f \alpha . Nw$$

$$= \frac{1}{2}(Cw + hkC0)V_{dd}^2 f \alpha . Nw$$

f is the frequency

N_w is the width of the wires

k is the number of optimum repeaters

h is the size of the repeaters.

C_0 is the input capacitance

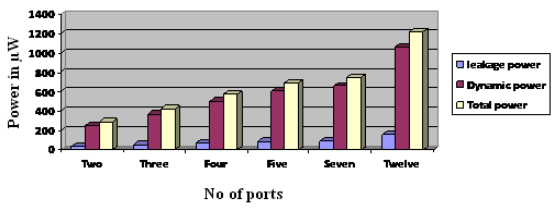
Where $k = \sqrt{\frac{0.4\, RintCint}{0.7R0C0}}$

and $h = \sqrt{\frac{Ro\ Cint}{Rint.C0}}$

Hence, the average global interconnection link power is given by

$$P_{link} = 0.875.Cw.V_{dd}^2 f \alpha . Nw \quad (2)$$

From the equation (1) and (2) for a given CTG, G= (V, E), the total power consumed by t he global interconnection links [13] is given by



(a)

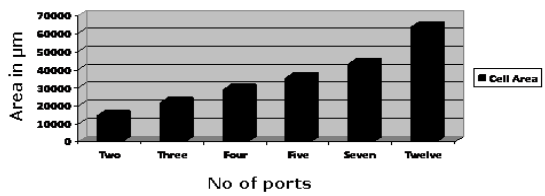
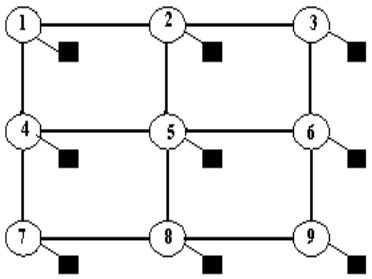


Figure 3 Comparison results for different number of port on 0.18 µm technology. (a) Power consumption (b) Area



(a)

B =

	1	2	3	4	5	6	7	8	9
1	0	1	2	1	2	3	2	3	4
2	1	0	1	2	1	2	3	2	3
3	2	1	0	3	2	1	4	3	2
4	1	2	3	0	1	2	1	2	3
5	2	1	2	1	0	1	2	1	2
6	3	2	1	2	1	0	3	2	1
7	2	3	4	1	2	3	0	1	2
8	3	2	3	2	1	2	1	0	1
9	4	3	2	3	2	1	2	1	0

(b)

Figure 4. (a) 3 X 3 Mesh topology (b) Connectivity matrix

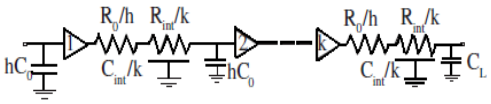


Figure 5. Optimal repeaters inserted in the interconnection link between router to router

$$P_{gl} = \frac{Psys\ .Plink}{Up} \quad (3)$$

This power modeling approximates only the dynamic power dissipation based on the traffic switching activity of the data packets transmitted from source to destination .This does not include the complete power dissipation after the physical placement and routing of the design. We used predictive Technology Model (PTM) to obtain the parameters for interconnection link using BSIM3 model from [18]. T he final network topology set must be such that P_{gl} is minimized. The parameters used for our evaluation [17] are given in table 1.

The total power consumed by the whole network topology including routers, the global interconnection links and the long range link is given by

$$Pt = \sum_{i=1}^{n} Pri + Pgl + \sum_{l=1}^{m} P_{longrangelink} \quad (4)$$

Where, P_r is the power consumed by the router and n is the number of cores in the application.

m is the number of long range link

The total power consumed by the whole network topology depends on the number of routers used and the power consumed by the global interconnection links which in turn depends on the number of links.

Proposed methodology

In this section we propose, a network partitioning algorithm that partitions the Communication task Graph (CTG) into three partitions to reduce the power consumption of the global interconnection links. In the proposed methodology three key steps are involved. First step is partitioning the CTG into three partitions, second, mapping the standard topologies onto three partitions and selecting the topology that consumes low power from each partition, and the final step is inserting long range link between the selected nodes of three partitions.

Table 1 Process Parameters

Technology	Vdd	Cw(fF/mm)
90nm	1.2	331

Table 2. Partitioned sets for MPEG-4 application based on the λ matrix entries using the proposed algorithm.

Partition 1	Partition 2	Partition 3
1, 2, 5, 9	3, 4, 6	7, 8, 10, 11, 12

Table 3. Comparison of MPEG-4 graph partitioning using two different methods.

Partitioning algorithm	Proposed Algorithm	Haythem Elmiligi
Global link power	4.9mW	6.7mW
Average number of hops	1	1.7

Table 4. Partitioned sets for PIP application based on the λ matrix entries using the proposed algorithm

Partition 1	Partition 2	Partition 3
2	1,5.6	3,4,7,8

Table 5. Comparison of the global link power for PIP application.

Partitioning algorithm	Global link power	Average number of hops
Proposed Algorithm	0.425mW	1
Haythem Elmiligi [13]	0.68mW	1.1

Step 1: Generating λ matrix from the CTG. Communication Task Graph (CTG). Here λij denotes the average number of packets transmitted per time period between the two cores.

Step 2: Apply network partitioning using the proposed algorithm.

We apply the network Partitioning algorithm to partition the CTG into three partitions in order to reduce the power consumption by reducing the cost of communication over the partitioned boundaries. Graph theoretical concept is applied for partitioning the CTG to reduce the number of cuts in the edges of the partition and minimize the interconnection traffic. A modified algorithm is developed for partitioning the graph. Before we apply the partition in the CTG, the cores level of connectivity is analyzed. Then long range link is inserted between the partitions to form the custom hybrid topology.

The proposed network partitioning algorithm:

1. Generate the Communication Distribution Matrix (CDM) from the core graph.
2. Check the rows one by one. Mark the row which has maximum number of non-zero entries as the seed cell 'Vi '.
3. If more than one row is present, then select the 'Vi' by trial and error.
4. In the 'Vi' row, select two columns that have largest entries. Mark them as 'Vj' and 'Vk'.
5. Here 'Vi', 'Vj' and 'Vk' form 3 different partitions.
6. Group all the nodes that are connected to Vj. If a node is already present in any other partition neglect it and continue grouping for the remaining nodes present in Vj.
7. Stop when no more nodes can be assigned.
8. Repeat steps 6 and 7 for row 'Vk'.
9. If the same node is present in 'Vj' and 'Vk', assign the node to any one partition such that the final the partitioned sets differ by ± 3 nodes.
10. Assign the unassigned nodes to 'Vi'

Step 3: Standard topology mapping on each partition.

We map each partition onto standard topologies and generate CDM λ for each partition. Followed by CDM generation, a unique connectivity matrix (B) is generated for each partition for all the mapped standard topologies. The power consumption P_{gl} for each topology in each partition is calculated using (3) and finally, the one topology that has low power consumption is selected from each partition.

Step 4: Insertion of long range link

In this step, a long range link is added between two selected nodes form each topology. The choice of the two nodes (v_i v_j) are selected such that the communication cost between these two nodes is maximum and is given by k=max (λ_{ij} , Bij) and the selected nodes are non neighbor. (5) The power calculation for the entire long range link is done using

$$P_{\text{long range link}} = 0.875.Cw.V_{dd}^{2}.f_{\alpha}.Nw \quad (6)$$

Finally, the total global power P_t for the whole network topology including global interconnection link, the long range link and the router is calculated using (4).

Evaluation of the proposed methodology

We evaluate the performance of the proposed methodology by an experimental case study for the benchmark video applications MPEG 4 decoder, PIP and VOPD. We use Matlab tool for the generation of connectivity matrix and the power calculation.

Evaluation of MPEG 4 decoder

This section explains the evaluation methodology for the application MPEG 4 video decoder.

Step 1: Generating the λ matrix from CTG

For the given CTG, The Communication Distribution matrix is generated. The CTG and the corresponding CDM λ matrix for MPEG-4 application are shown in the Fig 6. The numbers written on the arrows are the average number of packets/time step transmitted and the numbers on the circles are the PEs' numbers.

Step 2: Apply network partitioning using the proposed algorithm.

In this step, we follow the network partitioning algorithm proposed in step 2 of the section 5. The proposed algorithm is used to partition the graph into three partitions. Based on the entries of the Communication distribution matrix (λ) , the graph is divided into three partitions using the proposed algorithm. The partitioning process is performed until all the nodes are assigned to one of the three partitions keeping in mind that there is a balance of ±3 in the partition weights. Here we compare the results of the partition of the proposed algorithm with the algorithm of [13]. After applying the proposed algorithm, the partitioned sets obtained are as shown in Table 2. Figure 7

shows the partitioning applied to MPEG 4 decoder by using the proposed algorithm and the algorithm proposed by Haythem elmiligi [13].

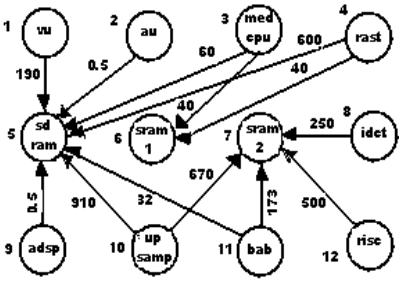
Step 3:Standard topology mapping on each partition.

We map each partition set onto standard topologies. Then for each topology a communication distribution matrix λ and connectivity matrix B are generated. Power calculations are done and the topology which has low power consumption is selected for each partition. In this case study, based on the power calculations results, the star topology is selected for the first PE-set (7,8,10,11,12) , the star topology is selected for the second PE-set (1,2,5,9) and a ring topology is selected for the third PE-set (3,4,6). The selected final topology is shown in figure 8(a). For comparison, the topology generated by Haythem Elmiligi [13] is shown in figure 8 (b). The global link power calculated by the proposed method and the method proposed by [13] are shown in table 3. The average number of hops is a calculation to measure the delay and power consumption. The average number of hops C_{av} is given by [13]

$$Cav = \frac{Ca}{Na}$$

Where ,

$$Ca = \sum_{i=1}^{n}\sum_{j=1}^{n} Cij\lambda ij \neq 0 \quad (7)$$

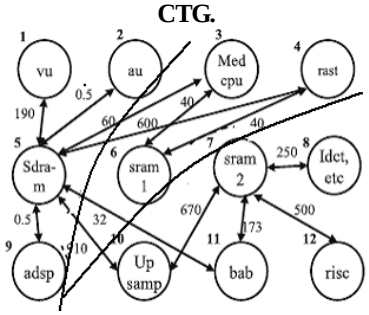


(a)

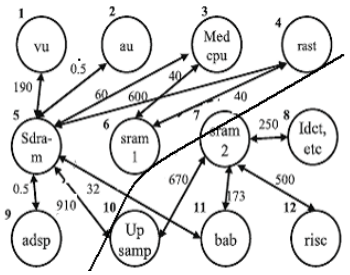
$$\lambda = \begin{bmatrix}
0 & 0 & 0 & 0 & 190 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0.5 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 60 & 40 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 600 & 40 & 0 & 0 & 0 & 0 & 0 & 0 \\
190 & 0.5 & 60 & 600 & 0 & 0 & 0 & 0 & 0.5 & 910 & 32 & 0 \\
0 & 0 & 40 & 40 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 250 & 0 & 670 & 173 & 500 \\
0 & 0 & 0 & 0 & 0 & 0 & 250 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0.5 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 910 & 0 & 670 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 32 & 0 & 173 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 500 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}$$

(b)

Figure 6(a) Communication Task Graph (CTG) for MPEG 4 (b) Communication Distribution matrix for MPEG 4 CTG.



(a)



(b)

Figure 7 MPEG-4 Decoder CTG: The cut line shows the partitioning boundary after applying the partitioning algorithm. Partitioning using (a) proposed algorithm, (b) Haythem Elmiligi algorithm [13].

Step 4: Inserting the long range link

In this step, we insert the long range link as stated in step 4 of section 5. Based on (5), we select the nodes 5,10,4 from each partition. Since maximum amount of packets are transmitted on these links. We connect each partition using long range link. The final topology after long range insertion is shown in figure 8.

Evaluation of PIP Application

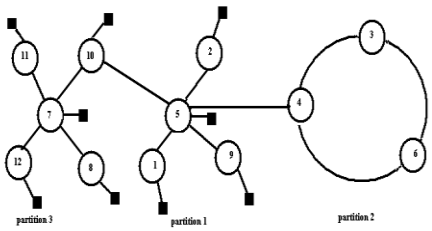
In this sub section, we evaluate the benchmark application PIP using the proposed algorithm. The results obtained by the proposed algorithm are superior both in global power consumption and the average number of hops compared to [13].

Step 1:Generating the λ matrix from CTG

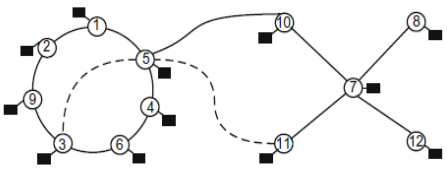
The Communication Task Graph, CTG and the corresponding Communication Distribution matrix, CDM λ matrix for PIP application are shown in the Fig 9. The numbers written on the arrows are the average number of packets/time step transmitted and the numbers on the circles are the PEs' numbers.

Step 2:Apply network partitioning using the proposed algorithm.

Here, we apply the proposed network partitioning algorithm to partition the CTG of PIP into three partitions. We follow the same procedures that are stated in step 2 of section 6.1. The partitioned Graph is shown in figure 10. For comparison we applied the algorithm proposed by [13] for the PIP CTG. After applying the proposed algorithm the partitioned sets are shown in table 4.

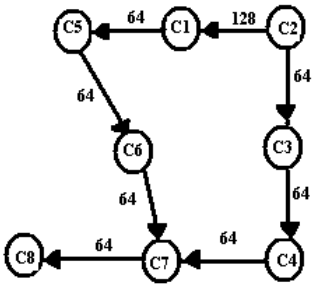


(a)



(b)

Figure 8. MPEG-4 application mapping to (a) Custom hybrid topology using the proposed method.(b) Custom hybrid method proposed by Haythem Elmiligi [13] approach. The dark line shows the long range link.



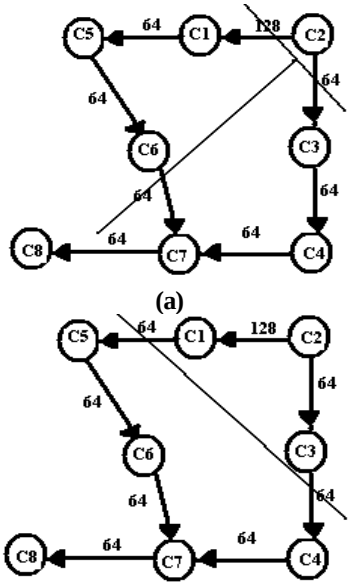
(a)

λ_{ij} =

	1	2	3	4	5	6	7	8
1	0	0	0	0	64	0	0	0
2	128	0	64	0	0	0	0	0
3	0	0	0	64	0	0	0	0
4	0	0	0	0	0	0	64	0
5	0	0	0	0	0	64	0	0

(b)

Figure 9 (a) Communication Task Graph (CTG) for PIP (b) Communication Distribution matrix λ for PIP CTG.



(a)

(b)

Figure 10 PIP CTG: The cut line shows the partitioning boundary after applying the partitioning algorithm. Partitioning using (a) proposed algorithm, (b) Haythem Elmiligi algorithm [13]

Step 3: Standard topology mapping on each partition.

We map each partition on to the standard topologies as stated in step 4 of section 6.1. In this case study, based on the power calculations results, we select ring topology for the partition set 2 (1,5,6) and mesh topology for the partition set 3 (3,4,7,8). For comparison we give the topology generated by applying the algorithm proposed by [13]. We worked on the power calculations and the average number of hops to the topology generated by [13] and the results are shown in table 5.

Step 4: Inserting the long range link

In this step, we insert the long range link to connect the partitions and to form the final topology. The insertion of the long range link satisfies the condition (5). The final topology after inserting the long range link is shown in figure 11.

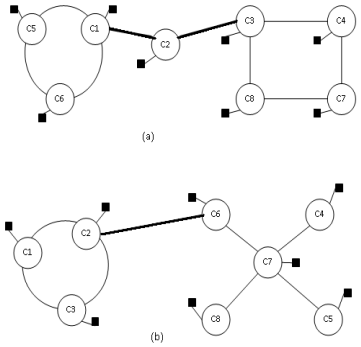


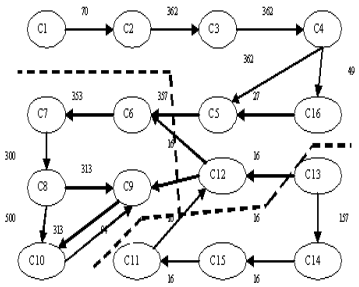
Figure 11. PIP application mapping to (a) Custom hybrid topology using the proposed method.(b) Custom hybrid method proposed by Haythem Elmiligi [13] approach. The dark line shows the long range link.

Evaluation of VOPD algorithm

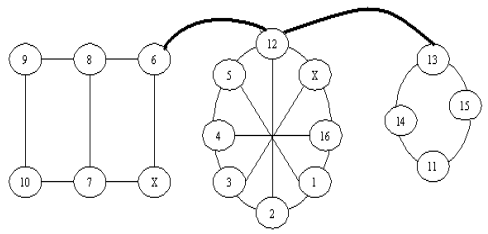
In this sub section, the proposed algorithm is applied to partition the VOPD (Video Object Plane Decoder) CTG. into three partitions to reduce the power consumption. Haythem Elmiligi [13] partitioning approach could not be used here since the constraint of ±2 difference in the balanced weight between the two partitioned sets could not be met here. The CTG and the final selected topology for VOPD application is given in figure 12.

Experimental results

In this sub section, we evaluate the efficiency of the proposed algorithm by performing the analysis to reduce the power consumption in global interconnection link and the routers. We perform the router power consumption analysis using 0.18µm technology for different number of ports. We also perform the power consumption of the global interconnection link and the average number of hops for various standard topologies , custom hybrid topologies generated by applying the proposed algorithm for benchmark applications MPEG 4 and PIP and the topology generated by [13]. The comparison results for the power consumption of the global interconnection link is shown in figure 13 and the comparison results for the average number of hops is shown in figure 14. The generated custom hybrid topology achieved the minimum global interconnection link power consumption, and less average number of hops compared to the approach of [13]. The global interconnection link power consumption is 26.8% less for MPEG 4 decoder and 37.5% for PIP application. The average number of hops is less 11.76% for MPEG 4 decoder and 9% for PIP application.

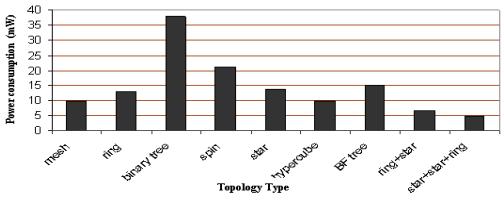


(a)

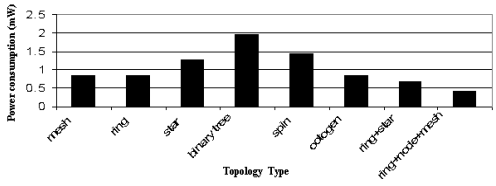


(b)

Figure 12. (a) The CTG of VOPD application (b) The final topology after applying the proposed algorithm. The dark line shows the long range link.

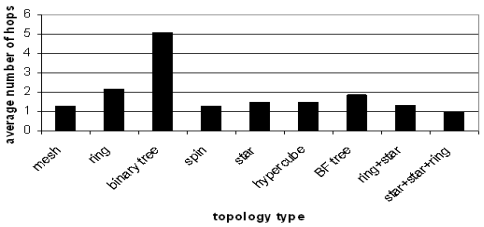


(a)

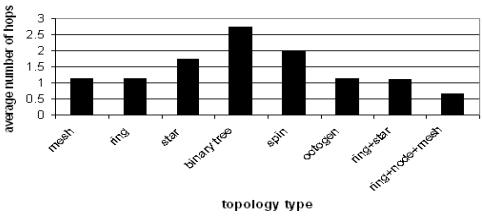


(b)

Figure 13 Comparison of the power consumption of global interconnection link between standard topologies, the topology generated in [13] and the topology generated by the proposed algorithm (a) for MPEG 4 decoder application (star+star+ring). (b) for PIP allocation (ring+node+mesh)



(a)



(b)

Figure 14 Comparison of the average number of hops between standard topologies , the topology generated in [13] and the topology generated by the proposed algorithm (a) for MPEG 4 decoder application (b) for PIP allocation

Conclusions and future work

A new partitioning algorithm to select the most favourable topology that achieves the lowest power consumption for a given application is presented in this section. The proposed algorithm partitions the given communication task graph into three and the three partitions are mapped onto the standard topologies. Then an optimum topology is selected for each partition that consumes low global interconnection power and long range links are inserted to connect the selected topologies. The efficiency of the proposed algorithm is validated through an experimental case study for the benchmark video applications MPEG 4 decoder, PIP and VOPD. The experimental case study shows26.8% and 37.5% of improvement in the power consumption for the applications MPEG 4 decoder and PIP respectively compared to the existing algorithm. We also achieve 11.76% and 9 % of improvement in average number of hops for the applications MPEG 4 decoder and PIP respectively compared to the existing algorithm.

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