Available online at www.elixirpublishers.com (Elixir International Journal)

Electrical Engineering

Elixir Elec. Engg. 57 (2013) 14080-14085

Elixir ISSN: 2229-712X

Single Network structure for Stuck-at and bridging fault Analysis and Diagnosis for Exclusive-OR Sum of Products in Reed-Muller Canonical Circuits

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ARTICLE INFO

Article history:
Received: 10 January 2013;
Received in revised form:
17 March 2013;
Accepted: 3 April 2013;

Keywords
Reed-Muller Canonical Form,
Exclusive-OR Sum of Products,
Testable Realization,
Single Stuck-at,
Double stuck-at,
AND-bridging fault,
OR-bridging fault.

ABSTRACT

In this paper, a testable design with good fault identification capability is used for analysis and diagnosis of stuck-at and bridging faults in Exclusive-OR Sum of Product Reed-Muller canonical circuits, independent of the function for a given number of inputs. Factors of identifiability and distinguishability have been defined and determined. Further, a compact method of representing the circuit outputs has been adopted for ease of tabulation and comparison. Simulations of Single stuck-at, Double stuck-at, OR-bridging and AND-bridging faults for a few random functions have been carried out through MATLAB coding. From the test results, it was found that the fault detection for the set of random functions was more than 95% for most of the functions except few cases, with just n+5 test vectors compared to 2^n test vectors required for conventional testing. The location of the fault can also be diagnosed through the output sets.

1. Introduction

The faults in digital circuits can be classified broadly as Single stuck-at-faults, Multiple stuck-at-faults, Stuck-open faults, stuck-on faults, Bridging faults, Path delay faults, Transient faults etc. Any arbitrary logic function, in general, can be expressed in Reed-Muller Canonical (RMC) form as

$F = (a_0 \oplus a_1x_1^* \oplus a_2\ x_2^* \oplus \ldots \oplus a_nx_n^* \oplus a_{n+1}\ x_1^*\ x_2^* \oplus \ldots \oplus a_m\ x_1^*\ x_2^* \ldots x_n^*)$

where, x_n^* can be x_n or its complement, a_n is either 0 or 1 and m = 2^n-1. However, there can be variations in such forms. The different types are Fixed Polarity RMC (FPRM), Positive Polarity RMC (PPRM), Generalised RMC (GRM) and Exclusive-OR Sum-of-Products (ESOP). The FPRM has a restriction that the variables in any of the product terms have to be of the same type namely complementary or non-complementary. For PPRM, the complementary form of variables is not allowed. The GRM may contain both complementary and non-complementary type but the combination of the variables should be unique. The ESOP form does not have any such restriction. Also the ESOP form has the least number of product terms and hence needs the least number of AND gates and is very much suitable for hardware implementation.

Extensive research has been carried out in the field of testing of digital circuits to reduce the number of input vectors. The cardinality of the test vectors proposed by many authors becomes prohibitively excessive for large number of input variables. It was demonstrated that Single stuck-at fault detection can be achieved with only n+5 test vectors [6]. The same structure was extended for OR-bridging fault analysis [15] and [16]. In this paper, it is shown through Matlab simulations for a few specific functions that Single stuck-at, Double stuck-at, OR-bridging and AND-bridging fault detection and diagnosis could also be achieved with the same n+5 test vectors considering all input lines, control lines and intermediate gate outputs.

Two quantitative indices, called identifiability factor and distinguishability factor are considered for comparison of the testability nature of given circuits. The identifiability factor is defined as the ratio of the number of faults correctly identified by the test set to the total number of possible faults of the type considered. The existence of faults can be recognized from the set of outputs measured which will be different from the fault-free circuit. The distinguishability factor pertains to the identical set of outputs among different faults, but the output set of each being very much different from the non-faulty case. The existence of even a large percentage of indistinguishability may not mean the circuit is not reliable, since it is still possible to identify the faulty condition of the circuit and take appropriate remedial action. The set of binary values for an output is converted into its decimal equivalent for convenience in comparison and ease of tabulation.

2. Literature Survey

A PPRM network for detection of stuck-at faults with a universal test set of size n+4, n being the number of data inputs, was proposed in [1]. Though quite good for self-testing, the method is economical only for the specified form, which obviously has more number of product terms than the other forms in most cases. Multiple stuck-at fault detection for ESOP circuits was carried out in [2]. However, since the cardinality is 2n+6+ $\sum nC_e$, e= 0 to j, the order of ESOP expression, the test set is not universal and also is too large to be practical for large input functions.

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Stuck-at and bridging faults with a universal test set for PPRM network has been reported in [3]. Multiple fault detecting GRM realizations was propounded in [4]. It was shown that 2n+s+3 test vectors, where s is the number of product terms in the logic function are required for Single stuck-at fault detections in GRM / ESOP circuits while 2n+s vectors are required for detection of AND/OR-bridging faults in such circuits [7]. Here too, the test set is not universal as it depends on s, the number of product terms of the function. [5] described an ESOP implementation with a universal test set of size n+6 for single stuck-at faults only. [6] demonstrated that Single stuck-at fault detection can be achieved with only n+5 minimal test vectors. [9, 10] proved that a test sequence of length (2n+8) vectors is sufficient to detect all Single stuck-at and bridging faults. Two methods, each with a small modification in this scheme with ESOP RMC circuits had been proposed for analysis and diagnosis of Single stuck-at faults [11, 12]. It was proved that test vectors for multiple fault detection and diagnosis in digital circuits could be generated using Neural Network with different training algorithms [8, 13, 18]. In [15, 16] it was demonstrated how the suitable RMC forms help in the detection of various digital faults. [19] proposed a new test pattern generation algorithm using Neural Network which requires additional gates. The analysis and diagnosis of OR-bridging faults in any of the pairs of data and control lines and OR-bridging faults including intermediate gate outputs of the ESOP RMC circuits was proposed in [20, 21].

This paper is an extension of [16], and discusses the analysis and diagnosis of Single stuck-at, Double stuck-at and AND-bridging faults including the intermediate gate outputs of the ESOP RMC circuits.

3. Materials and methods

3.1 Network Structure:

The network structure of the scheme is the same as that proposed in [6] and is shown in Figure.1. It comprises literal complementing XOR block, an AND block, an XOR function tree block, which implements the required logic function as also two additional outputs O_1 and O_2 obtained through a separate AND gate and an OR gate. The actual data inputs to the system are x_1, x_2 …. x_n. Additionally, the scheme requires four control inputs c_1 to c_4. The literal-complementing block produces the complements of the literals used in the function. Only those literals appearing in complemented form require an XOR gate in this block.

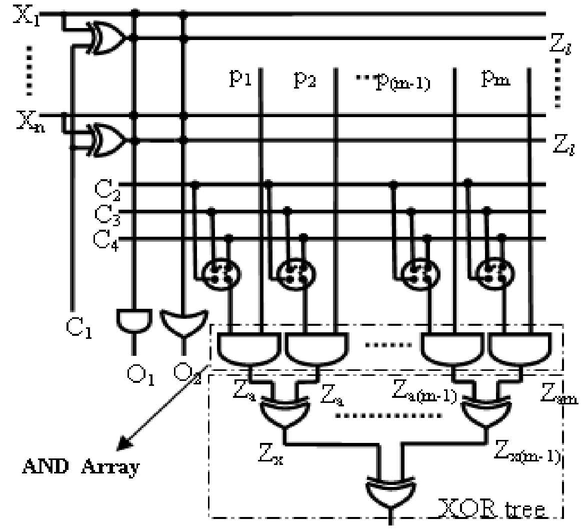


Figure 1. Generalized Network Structure

The literals of each product term are combined through an AND gate and hence the number of AND gates required is the same as the number of product terms in the logic function. Further, each of the AND gates of this block has an additional input from one of the control lines depending on the number of gates used in the XOR tree block producing the final function F. Finally, all the data and complementary gate outputs are applied to a separate AND gate and an OR gate, producing auxiliary outputs O_1 and O_2, to aid in the detection of faults which cannot be differentiated by the main function output F alone.

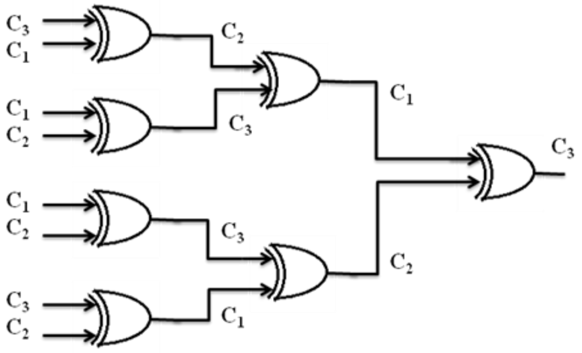


Figure. 2. Control Input Determination

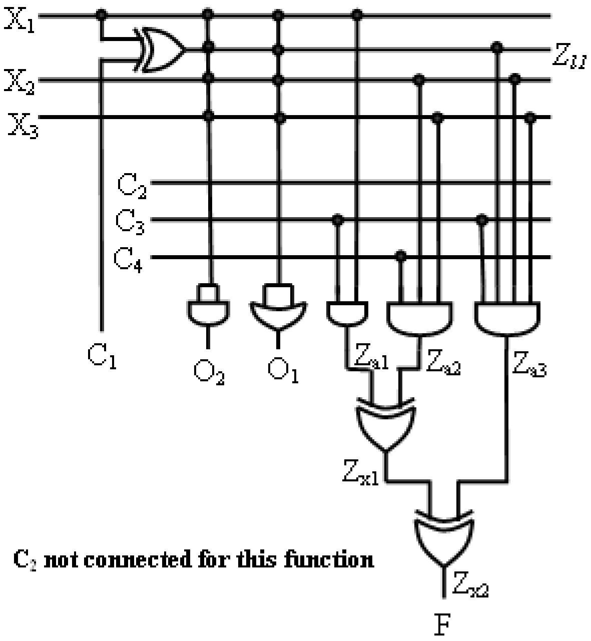
The required control lines are determined as illustrated above (Figure 2). Draw the XOR gate tree for the required product terms of the given function. Assign the numerals 1, 2 and 3 respectively to the two inputs and the output of the final XOR gate producing the function output F. Consider each XOR gate connected to the inputs of the final XOR gate considered. Assign the outputs of these XOR gates with the same numbers as the inputs of the final XOR gate. If the output of the XOR gate considered is 1, then assign 2 and 3 to its inputs. Else if the output is numbered 2, assign 3 and 1 to its input. Now consider the next earlier input stage and assign the numerals in the similar manner according to the output points connected.

3.2 Test Vectors:

The test set has (n+5) vectors; each of the vectors is (n+4) long, ‘n’ being the number of data inputs. The first four columns of the matrix represent the control inputs c_1 to c_4 while the remaining n columns that of the data inputs are x_1 to $x_{n.}$ The generalized test set is shown in Table 1.

Table 1. Generalized Test Set

$$T = \left\{ \begin{array}{cccccccc}
c_1 & c_2 & c & c_4 & x_1 & x_2 & \ldots & x_n \\
0 & 0 & 0 & 0 & 0 & 0 & ... & 0 \\
0 & 0 & 1 & 1 & 1 & 1 & ... & 1 \\
0 & 1 & 0 & 1 & 1 & 1 & ... & 1 \\
0 & 1 & 1 & 1 & 1 & 1 & ... & 1 \\
0 & 1 & 1 & 1 & 0 & 1 & ... & 1 \\
0 & 1 & 1 & 1 & 1 & 0 & \ldots & 1 \\
0 & 1 & 1 & 1 & 1 & 1 & \ldots & 1 \\
. & . & . & . & . & . & & \\
. & . & . & . & . & . & & \\
. & . & . & . & . & . & & \\
0 & 1 & 1 & 1 & 1 & 1 & ... & 0 \\
1 & 0 & 0 & 0 & 0 & 0 & ... & 0
\end{array} \right\}$$



C₂ not connected for this function

Figure. 3. Circuit for F= $x_1\oplus x_2x_3\oplus x_1'x_2x_3$

The network structure and the set of test vectors for the function F= $x_1\oplus x_2x_3\oplus x_1'x_2x_3$ are shown in Figure.3 and Table 2 respectively.

Table 2. Test vectors for F= $x_1\oplus x_2x_3\oplus x_1'x_2x_3$

$$T = \left\{\begin{array}{ccccccc} c_1 & c_2 & c_3 & c_4 & x_1 & x_2 & x_3 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 1 & 1 & 1 \\ 0 & 1 & 0 & 1 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 1 & 1 & 0 & 1 \\ 0 & 1 & 1 & 1 & 1 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{array}\right\}$$

3.3 Algorithm

Step 1: Set up the circuit as in Figure.2.

Step 2: Determine and connect the control lines c_1 to c_4 as explained.

Step 3: Apply the test vectors as given in Table 2, one by one.

Step 4: For each test vector, determine the fault free outputs F, O_1 and O_2.

Step 5: Obtain the decimal equivalents of each of the above binary output sets.

Step 6: Simulate the Single stuck-at fault at the control input, data input and intermediate gate outputs and get the corresponding decimal outputs.

Step7: Compare the set of outputs with the predetermined fault-free condition outputs

Step 8: If the two output sets match exactly, it implies that a fault, if present, is not identifiable or detectable; else, the fault is a detectable one.

Step 9: Repeat steps 4 to 8 for Double stuck-at, OR-bridging and AND-bridging fault for other possible combination pairs of control inputs, data inputs and intermediate gate outputs in the network.

Step 10: For all the faults, the identifiability factor and distinguishability factor are calculated as explained above.

4. Results and Discussion

The following ten random functions were considered and Single stuck-at, Double stuck-at, OR-bridging and AND-bridging faults are simulated using MATLAB coding and the results are tabulated in Table 5, 6, 8 and 9.

$F_1 = x_1\oplus\square x_2x_3\oplus\square\square x_1'x_2x_3$

$F_2= x1x2\oplus\square x_2'x_3\oplus\square\square x_3'x_4\oplus\square\ x_1x_2x_3$

$F_3= x1'\oplus\square\square x_2x_3'x_4\oplus\square\square x_3x_4'\ \oplus\square\square x_2'x_3\oplus\square\square x_1x_4x_5$

$F_4=x_1x_2'$
$\oplus\square\square x_2x_3x_4\oplus\square x_4x_5'x_6\oplus\square\square x_2x_5\square\oplus\square\square x_2'x_5'\oplus\square\square x_3'x_2x_1\oplus\square\square x_4x_6$

$F_5 = x_1'x_2x_3\oplus\square\square x_4x_5x_6\square\oplus\square\square x_4'x_6'x_7\square\oplus\square\square x_3x_5x_7$

$F_6=x_1x_2'x_3\oplus\square\square x_4'x_5x_6'\square\oplus\square\square x_7x_8'\square\square\oplus\square\square'$
$\oplus\square\square x_1'x_6\square\oplus\square\square x_3'x_4\oplus\square\square x_1x_5\square$
$\oplus\square x_4x_5'\square\oplus\square\square x_5x_7\square\oplus\square\square x_8x_3x_1\square\oplus\square\square x_3x_5'x_8$

$F_7 = x_1x_2'x_3'$
$\oplus\square\square x_4x_5'x_6\oplus\square\square x_7'x_8x_9\square\oplus\square\square x_1'x_4'x_9'\square\oplus\square x_2x_5'\square\oplus\square\square x_3x_5$

$F_8 = x_1'x_2x_3'\ \oplus\square\square x_4'x_5'x_6\oplus\square\square x_7x_8'x_9'$
$\oplus\square\square x_{10}\square\oplus\square\square x_6'x_7\oplus\square\square x_8x_{10}$

$F_9 =$
$x_1\oplus\square\square x_2'x_3x_4'\oplus\square\square x_5'x_6x_7'\oplus\square\square x_8x_9x_{10}\square\oplus\square\square x_{10}'x_{11}\square\oplus\square\square x_1x_3x_9$

$F_{10}=x_1'x_2\oplus\square\square x_3x_4'x_5\oplus\square\square x_6x_7'x_8x_9\oplus\square\square x_{10}x_{11}'x_{12}\square\oplus\square\square x_1x_2x_3'\square\oplus$
$\square\square x_4'x_7$

4.1 Single Stuck-at fault

As an illustration, a three variable function

$F_1 = x_1\oplus\square x_2x_3\oplus x_1'x_2x_3$ is considered. The simulated fault-free output set was found to be {F, O_1, O_2} = {126, 112, 127}. The stuck-at-0 and stuck-at-1 faults are simulated for the given function at lines c_1, c_2, c_3, c_4, x_1, x_2 , x_3, zl_1, za_1, za_2, za_3, zx_1 and zx_2 and the results are shown in Table 3 and 4.

Table 3. Stuck-at-0 for 3 variable functions

	c_1	c_2	c_3	c_4	x_1	x_2
F	126	126	120	6	120	86
O_1	112	112	112	112	0	0
O2	126	127	127	127	127	127

	x_3	z l_1	za_1	za_2	za_3	zx_1	zx_2
F	86	46	40	6	46	80	0
O_1	0	0	112	112	112	112	112
O_2	127	126	127	127	127	127	127

Table 4. Stuck-at-1 for 3 variable functions

	c_1	c_2	c_3	c_4	x_1	x_2
F	38	126	126	126	126	126
O_1	0	112	112	112	120	116
O2	255	127	127	127	255	255

	x_3	z l_1	za_1	za_2	za_3	zx_1	zx_2
F	126	118	215	249	209	175	255
O_1	114	112	112	112	112	112	112
O2	255	255	127	127	127	127	127

The total number of possible single stuck-at faults are 2*(nc+nx+zl+za+zx) = 2*13 = 26.

Where nx is the number of data inputs
nc is the number of control inputs
zl is the number of complementary functions
za is the number of AND gate outputs
zx is the number of XOR gate outputs

For stuck-at-0 fault at c_2 and for stuck-at-1 fault at c_2, c_3 and c_4 the output sets obtained are same as that of fault free one. Hence, these faults are unidentifiable. The identifiability factor = (26-4)/26100 = 84.62%. Also, in stuck-at-0 fault the output set {6, 112, 127} is repeated two times for c_4 and za_2 and {86, 0, 127} is repeated two times for x_2 and x_3.

These faults are indistinguishable. The distinguishability factor for this set is (26-4)/ 26 *100= 84.62%

The simulated results for the ten random functions are tabulated in Table 5.

Table 5. Simulation results for Single stuck-at fault

S.No.	Function	No. of data Inputs	Total Possible Faults	Identifiability Factor (%)	Distinguishability Factor (%)
1	F_1	3	26	84.62	84.62
2	F_2	4	34	97.06	82.35
3	F_3	5	44	95.45	95.45
4	F_4	6	54	96.30	92.59
5	F_5	7	42	97.62	73.81
6	F_6	8	82	96.34	97.56
7	F_7	9	62	98.39	83.87
8	F_8	10	64	98.44	78.13
9	F_9	11	62	98.39	79.03
10	F_{10}	12	64	98.44	78.13
Average	96.11	84.55			

4.2 Double Stuck-at faults

Double Stuck-at faults can occur quite easily due to the shorting of any two of the lines, especially the adjacent lines of the circuit.

The network structure and test vectors are the same as those for the single stuck-at fault. However, in the test procedure, two lines at a time are considered and made to stuck-at-0 or stuck-at-1 and simulated. Since two lines are involved, four possible combinations, viz. (0,0), (0,1), (1,0) and (1,1) are simulated and tabulated in Table 6.

Table 6. Simulation results for Double stuck-at fault

S.No.	Function	No. of data Inputs	Total Possible Faults	Identifiability Factor (%)	Distinguishability Factor (%)
1	F_1	3	312	98.40	30.13
2	F_2	4	544	100	31.25
3	F_3	5	924	99.89	33.98
4	F_4	6	1404	99.93	33.26
5	F_5	7	840	100	29.64
6	F_6	8	3280	100	32.50
7	F_7	9	1860	100	32.80
8	F_8	10	1984	100	31.50
9	F_9	11	1860	100	33.12
10	F_{10}	12	1984	100	31.10
Average				99.82	31.93

4.3 AND-Bridging Faults

The bridging faults are considered as a special case of multiple faults. The AND-bridging fault is simulated by shorting two lines at a time. A detailed numerical illustration for three variable AND-bridging faults is given below.

Function considered: $F_1 = x_1\oplus□x_2x_3\oplus□x_1'x_2x_3$

Fault-free output set $\{F, O_1, O_2\} = \{126, 112, 127\}$

The outputs of AND-bridging faults at lines c_1 in combination with c_2, c_3, c_4, x_1, x_2 , x_3, zl_1, za_1, za_2, za_3, zx_1 and zx_2 are tabulated in Table 7.

Table 7. Simulation Results for a few Random Logic Functions

	c_1 c_2	c_1 c_3	c_1 c_4	c_1 x_1	c_1 x_2	c_1 x_3
F	126	120	6	120	86	86
O_1	112	112	112	0	0	0
O_2	126	126	126	126	126	126

	c_1 zl_1	c_1 za_1	c_1 za_2	c_1 za_3	c_1 zx_1	c_1 zx_2
F	46	40	6	46	80	0
O_1	0	112	112	112	112	112
O_2	127	126	126	126	126	126

Control inputs: c_1 to c_4; Data inputs: x_1 to x_3
Complementary outputs: zl1; AND gate outputs: za_1, za2, za_3XOR gate outputs: zx1 & zx2
Total No. of Fault location pair combinations
= (nc+ nx+zl+za+zx) C_2= 13C_2=78

Total number of possible bridging faults for the given three variable function used is 78.

When the Post fault outputs are identical as of fault free one, then those faults are termed as unidentifiable faults. From the simulation results it was found that the number of unidentifiable faults as 11.

$\therefore$The Identifiability Factor is (78-11)/ 78x100 = 85.90%.

When the post fault outputs are same for different combinations of faults, then those faults are termed as Indistinguishable faults. For the given example, the output sets that get repeated are as follows:

{6, 112, 126}	2 times
{62, 112, 127}	5 times
{80, 112, 127}	2 times
{80, 112, 127}	2 times
{86, 0, 126}	2 times
{86, 80, 127}	2 times
{86, 112, 127}	5 times
{94, 112, 127}	2 times
{118, 112, 126}	5 times
{118, 112, 127}	2 times
{120, 112, 127}	4 times
{126, 48, 127}	3 times
{126, 80, 126}	3 times
{126, 80, 127}	2 times

Thus totally repetition occurs for 41 fault location combinations. Hence overall distinguishability factor is
(78-41) /78 x100 = 47.44%

However, when the individual cases are considered the distinguishability factor can be seen to be appreciably high as seen below:

Same output set of {120, 112, 127} for the following fault combinations.

AND-bridging fault at $c_{3,}$ za_3 lines
AND-bridging fault at $za_{1,}$ za_3 lines
AND-bridging fault at $za_{2,}$ zx_1 lines
AND-bridging fault at $za_{2,}$ zx_2 lines

The distinguishability for this set is
(78-4)/ 78 x100= 94.87%.

Similarly, the output set {126, 80, 126} occurs 3 times, for which the distinguishability factor is
(78-3)/78x100 = 96.15%.

Further, the location of fault can also be easily diagnosed from the output set. For instance if the output set is {120, 112, 127} then the fault condition would be one of the four cases discussed above involving c_3, $za_{1,}$ $za_{2,}$ $za_{3,}$ $zx_{1,}$ zx_2 and hence those lines only need to be checked.

Similarly, the fault simulations were carried out for the remaining nine random functions and the results are tabulated in Table 8.

Table 8. Simulation results for AND-bridging faults

S.No.	Function	No. of Data Inputs	Total Possible Faults	Identifiability Factor (%)	Distinguishability Factor (%)
1	F_1	3	78	85.90	47.44
2	F_2	4	136	95.59	36.76
3	F_3	5	231	89.18	47.62
4	F_4	6	351	90.88	52.42
5	F_5	7	210	86.19	48.10
6	F_6	8	820	91.59	58.66
7	F_7	9	465	91.40	47.74
8	F_8	10	496	90.52	33.06
9	F_9	11	465	90.75	38.49
10	F_{10}	12	496	89.11	47.98
Average				90.11	45.83

4.4 OR-Bridging Faults

The OR-bridging fault is simulated considering two lines at a time with all possible combinations of control lines, data lines and intermediate gate outputs. The simulated results for ten random functions are given in Table 9.

Table 9. Simulation results for OR-bridging faults

S.No.	Function	No. of Data Inputs	Total Possible Faults	Identifiability Factor (%)	Distinguishability Factor (%)
1	F_1	3	78	84.62	58.97
2	F_2	4	136	98.53	52.21
3	F_3	5	231	96.54	59.74
4	F_4	6	351	96.58	67.24
5	F_5	7	210	98.57	85.71
6	F_6	8	820	98.29	70.12
7	F_7	9	465	98.28	79.14
8	F_8	10	496	98.59	85.89
9	F_9	11	465	98.71	86.88
10	F_{10}	12	496	98.79	80.85
Average				96.75	72.68

From the test results as given in Table 5, 6, 8 and 9, it was found that the identifiability factor for the set of random functions tested through MATLAB simulation was more than 95% for all the functions of Single stuck-at, Double stuck-at, and OR-bridging types of faults except AND-bridging faults, with just n+5 test vectors compared to 2^n test vectors required for conventional testing. It was also observed that even though the overall distinguishabililty factor was in the range of 31-85%, the individual set distinguishability factor was more than 93% as explained above.

Though the overall distinguishability is small, it does not affect the detection capability. Further, the distinguishing capability for an individual output set can be quite high, as illustrated above.

5. Conclusion

A test set scheme for detection of Single stuck-at, Double stuck-at, OR-bridging and AND-bridging faults for ESOP RMC logic functions have been detailed and the simulation results are shown. The results conclude that n+5 test vectors can be used to detect Single Stuck-at, Double stuck-at, OR-bridging and AND-bridging faults in digital circuits. Further, the location can also be diagnosed through the output set. The analysis and diagnosis have been done through compact tabulation and two quantification indices. All possible combinations of the data lines, control lines and all intermediate gate outputs line pairs have been considered. Detection factor and Distinguishability factor can be further improved by modifying the network structure or using different test vectors.

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