

## Cascaded H-bridge inverter with reduced number of switches and a single dc source

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### ABSTRACT

This paper presents a new topology for a seven-level cascaded H-bridge multilevel inverter. The proposed topology uses reduced number of switches and requires only one DC source. The new topology results in reduced cost and can be implemented for any number of levels. The proposed seven-level inverter is simulated in MATLAB-Simulink. The switching angles are generated using a new technique of selective harmonic elimination technique. The simulated waveforms of output voltage have reduced total harmonic distortion.

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### Introduction

Multilevel inverters (MLIs) are used in renewable energy applications for boosting low source voltage to higher voltage for transmitting power to loads and/ or to grid. They have higher efficiency, lower electromagnetic interference effects, lower switching losses, reduced output  $dv/dt$ , higher voltage capability and better power quality as compared to conventional inverters [1-3]. There are mainly three configurations of MLIs namely Cascaded H-Bridge, Neutral Point Clamped and Flying Capacitor. Of these the Cascaded H Bridge (CHB) Inverter has proven to be a better for high power applications as it does not require any clamping diodes or capacitors. It achieves the high voltage by cascading multiple single-phase inverter modules and requires the least number of components [4-6]. The main disadvantage of the CHB inverter is that it requires a separate DC sources for each level. All three inverter configurations require more number of switches, which further increases with increase in the number of levels. This paper proposes a new topology for CHB MLI, which uses only two switches per level and a single DC source. The inverter is simulated in MATLAB-Simulink environment with switching angles being decided by the selective harmonic elimination method.

### Conventional CHB Inverter

The conventional CHB inverter uses identical H-bridges in cascade. The output voltage waveform is more sinusoidal and hence the THD value is less with the increase in H bridges. For an  $n$ -level inverter, there are  $(n-1)/2$  identical H-bridges. There must be a separate DC source for every individual H-bridge [7]. Fig. 1 shows the conventional single-phase seven-level CHB. The inverter uses three separate DC sources. Each DC source has a single-phase H-bridge inverter with four switches resulting in twelve switches for the seven-level inverter. Fig. 2 shows the output voltage waveform of the seven level inverter. The seven levels of voltages are  $0, \pm V_{DC}, \pm 2V_{DC}$  and  $\pm 3V_{DC}$ .

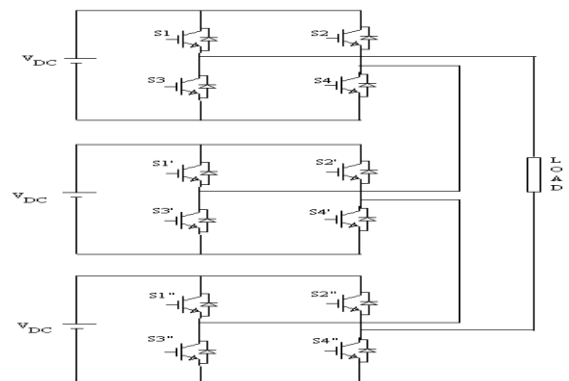


Figure 1. Circuit of Conventional Seven-level CHB Inverter

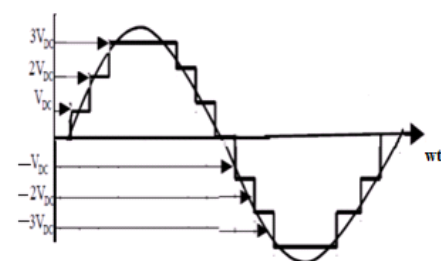
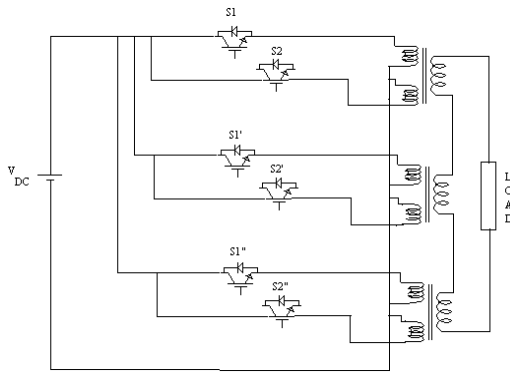


Figure 2. Output Voltage of a Seven-level Inverter Proposed Multi-Level Inverter

Fig. 3 shows the proposed topology of the CHB multi-level inverter. The inverter requires only  $(m-1)$  switches for  $m$ -level, hence only six switches are required to implement the seven-level inverter. It requires only one DC source. It uses 3 three winding transformers with two primary windings and one secondary winding. The DC source is connected to the primary side of the transformer through the switches. The secondary windings are connected in series and the load is connected to the series connected secondary windings. The switching states to get the seven levels of output voltages are given in Table 1.

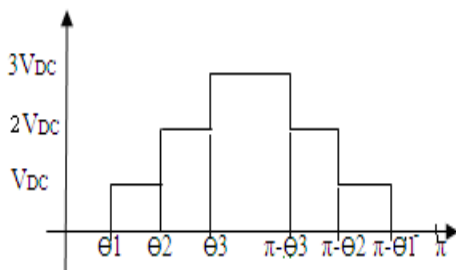


**Figure 2. Circuit of Proposed Seven-level CHB Inverter**  
**Table 1 Switching States For The Proposed Seven Level Inverter**

Output voltage	S1	S2	S1'	S2'	S1''	S2''
$+V_{DC}$	ON	OFF	OFF	OFF	OFF	OFF
$+2V_{DC}$	ON	OFF	ON	OFF	OFF	OFF
$+3V_{DC}$	ON	OFF	ON	OFF	ON	OFF
0	OFF	OFF	OFF	OFF	OFF	OFF
$-V_{DC}$	OFF	ON	OFF	OFF	OFF	OFF
$-2V_{DC}$	OFF	ON	OFF	ON	OFF	OFF
$-3V_{DC}$	OFF	ON	OFF	ON	OFF	ON

**Switching Signals for the Inverter using Selective Harmonic Elimination Method**

The multi-level output AC voltage is obtained by switching ON and OFF the semiconductor switches in such a way that the desired fundamental is obtained with less harmonic distortion. The commonly used technique for switching is the selective harmonic elimination (SHE) method at fundamental frequency. In this technique, the switching angles are computed by solving transcendental equations characterizing harmonics [8-9]. For a seven-level inverter, three switching angles are to be generated by solving three transcendental equations. These equations are solved using Newton-Raphson method, which is one of the fastest iterative methods. This method solves the transcendental equations with initial approximate values [10].



**Figure 4. Output Voltage of the Seven-Level Inverter with Switching Angles for a Half-Cycle**

The output voltage waveform of the seven-level inverter is shown in Figure 4 for a half-cycle. This staircase waveform can be expressed using Fourier series as given by Eqn. 1.

$$v_a(\omega t) = \sum_{n=1,3,5}^{\infty} \frac{4V_{DC}}{n\pi} (\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3)) \sin(n\omega t) \tag{1}$$

Where  $\theta_1, \theta_2,$  and  $\theta_3$  are the switching angles for the seven-level inverter, and  $0 < \theta_1 < \theta_2 < \theta_3 < \pi/2$ . From Eqn.1 the fundamental voltage is given by Eqn. 2 [11].

$$V_1 = \frac{4V_{DC}}{\pi} (\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3)) \tag{2}$$

The maximum value of the fundamental voltage is

$$V_{m1} = \frac{4V_{DC}}{\pi}, \text{ i.e., the value of the fundamental voltage when}$$

all the switching angles are zero. Modulation index  $M_I$  is the ratio of fundamental voltage to maximum fundamental voltage.

$$M_I = \frac{V_{DC}}{V_{m1}}. \text{ Three equations can be formed to eliminate third}$$

and fifth harmonics, as given by Eqns. 3-5[12].

$$\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) = M_I \tag{3}$$

$$\cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3) = 0 \tag{4}$$

$$\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) = 0 \tag{5}$$

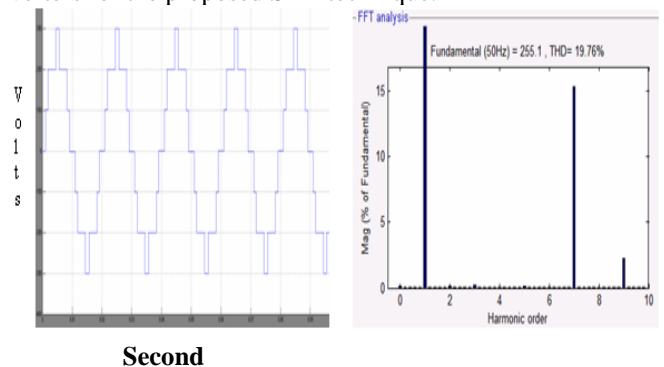
Solving these equations by Newton-Raphson method, the switching angles are found to be  $\theta_1 = 0.2923$  rad,  $\theta_2 = 0.5542$  rad,  $\theta_3 = 1.377$  rad for  $M_I = 2$ . Hence the third and fifth harmonics are eliminated, while higher order harmonics are present. This paper considers a new technique for the minimisation of seventh harmonic in addition to the elimination of third and fifth harmonics. This is implemented by considering seventh harmonic equation along with the third and fifth harmonic equations and ignoring the fundamental one. Seventh harmonic cannot be completely eliminated but can be minimised by equating Eqn. 6 to a minimum value.

$$\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) = 0.0001 \tag{6}$$

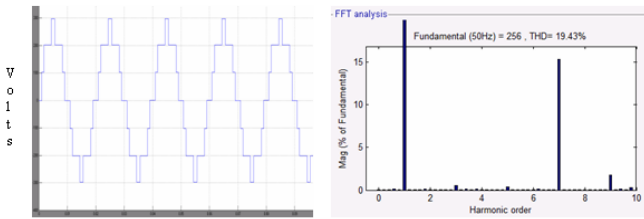
By solving Eqns. 4-6 by Newton-Raphson method, the values of switching angles are found to be  $\theta_1 = 0.2037$  rad,  $\theta_2 = 0.4701$  rad,  $\theta_3 = 0.9784$  rad.

**Simulation and Results**

The conventional seven-level CHB inverter and the proposed CHB inverter are simulated in MATLAB-Simulink with switching angles generated by the usual SHE and the proposed SHE techniques. The waveforms of the output voltages obtained are shown for the two configurations. Figures 5 and 6 show the simulated output voltage of conventional and proposed inverters for conventional SHE technique. Figures 7 and 8 show the simulated output voltage of conventional and proposed inverters for the proposed SHE technique.



**Figure 5. Output voltage and FFT analysis of conventional CHB inverter with the conventional SHE technique**



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Figure 6. Output voltage and FFT analysis of proposed CHB inverter with the conventional SHE technique

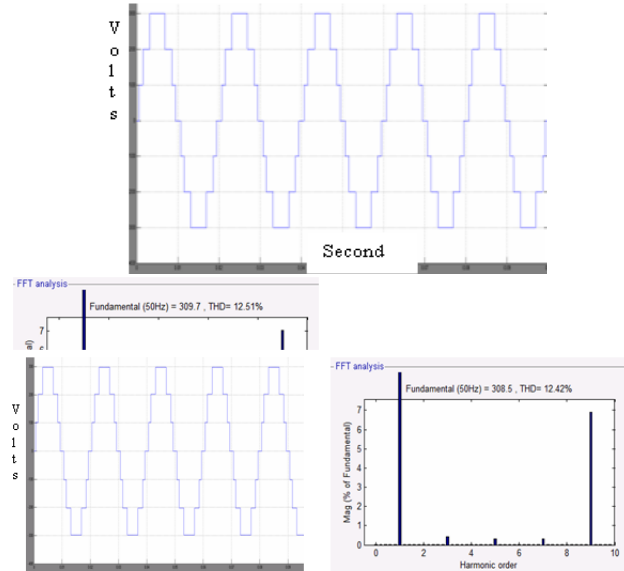


Figure 8. Output voltage and FFT analysis of proposed CHB inverter with the proposed SHE technique

From Figs. 5 and 7, it is found that the voltage THD of the conventional inverter is found to be 19.76% for the conventional SHE and 12.51% for the proposed SHE technique. From Figs. 6 and 8, it is found that the voltage THD of the proposed inverter is found to be 19.43% for the conventional SHE and 12.42% for the proposed SHE technique.

**Comparison of the Conventional Inverter with the Proposed Inverter**

Table 2 shows the comparison of the seven level conventional inverter with the proposed inverter. From the table it is found that the number of switches required for the proposed one is less than the conventional one and the proposed topology requires only one DC source but the conventional inverter requires (m-1)/2 DC sources for m level inverter. Hence the cost involved is less for the proposed one.

**Table 2. Comparison of Various Parameters of Seven-Level Conventional and Proposed CHB inverter**

Inverter	No. of switches	No of DC sources	Voltage THD with the conventional SHE	Voltage THD with the proposed SHE
Conventional CHB inverter	12	3	19.76%	12.51%
Proposed CHB inverter	6	1	19.43%	12.42%

**Conclusion**

This paper presented a new topology for CHB inverter which uses less number of switches compared to conventional multi-level inverter. The proposed inverter uses only (m-1) switches whereas the conventional inverter uses 2(m-1) switches, for an m-level inverter. In addition, the proposed topology uses only one DC source irrespective of the levels but the conventional one uses (m-1)/2 DC sources for m level,

resulting in reduced cost of the proposed inverter. This paper also presented a new technique for SHE, which involves the elimination of third and fifth and reduction of seventh harmonics resulting in lower THD value.

**References**

[1] Jih-Sheng Lai and Fang Zheng Peng, "Multilevel Converters - A New Breed of Power Converters", IEEE Transactions on Industry Applications, Vol. 32, No. 3, pp. 509-517, May/June 1996.

[2] F. Z. Peng, J. W. McKeever and D. J. Adams, "Cascade Multilevel Inverters for Utility Applications", IECON Proceedings (Industrial Electronics Conference), Vol. 2, pp. 437-442, 1997.

[3] B. Urmila and D. Subbarayudu, "Multilevel Inverters: A Comparative Study of Pulse Width Modulation Techniques", International Journal of Scientific & Engineering Research, Vol. 1, No. 3, pp. 1-5, December 2010.

[4] José Rodríguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel Inverters: A Survey of Topologies", IEEE Transactions on Controls and Applications, Vol. 49, No. 4, August 2002.

[5] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari and G. Sciuotto, "A New Multilevel PWM Method: A Theoretical Analysis", IEEE Transactions on Power Electronics, Vol. 7, No. 3, pp.497-505, July 1992.

[6] T. Porselvi and R. Muthu, "Comparison of Cascaded H-Bridge, Neutral Point Clamped and Flying Capacitor multilevel inverters using multicarrier PWM", INDICON 2011-Annual IEEE India Conference, Hyderabad, India, December 16-18.

[7] T. Prathiba and P. Renuga, "A comparative study of Total Harmonic Distortion in Multi level inverter topologies", Journal of Information Engineering and Applications, Vol. 2, No.3, pp. 26-36, 2012.

[8] Fang Zheng Peng, Jih-Sheng Lai, J. McKeever and J. Van Coevering, "A Multilevel Voltage-Source Inverter with Separate DC Sources for Static Var Generation", IEEE Trans. on Industry Applications, Vol. 32, No. 5, pp. 1130-1138, September/October 1996.

[9] Jose Rodriguez, J S Lai, and F. Z. Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications", IEEE Trans. on Industrial Electronics, vol. 49, no. 4, pp. 724-738, August 2002.

[10] C. Woodford and C. Phillips, "Numerical Methods with Worked Examples", Chapman and Hall, pp. 45-57, First edition 1997.

[11] Jagdish Kumar and Biswarup Das, "Selective Harmonic Elimination Technique for a Multilevel Inverter", Fifteenth National Power Systems Conference (NPSC), IIT Bombay, pp. 608-61, December 2008.

[12] C. Udhaya Shankar, J.Thamizharasi, Rani Thottungal, N. Nithyadevi, "Harmonic Reduction in Cascaded Multilevel Inverter with reduced number of switches with Genetic Algorithm", International Journal of Advances in Engineering & Technology, Vol. 3, Issue 1, pp. 284-294, March 2012.

[13] Aniket Anand, K.P.Singh, "Selective Harmonics Elimination of PWM Cascaded Multilevel Inverter", International Journal of Engineering Science and Technology, Vol. 4, No.06 June 2012, pp.2743-2747.

[14] M. K Maharana, Rupali Mohanty, "PSO based Harmonic Reduction Technique for Wind Generated Power System", Special Issue of International Journal of Power System Operation and Energy Management, Volume - 1, Issue-3, pp. 100-104.