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A double dual slope analog divider

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ABSTRACT

A Novel type of analog divider is described. The circuit enables division of a dc voltage with another dc voltage. The constant of division is dependent upon two resistor values. Employing precision resistors, an acceptable level of accuracy can be obtained in the division. Verification of the feasibility of the circuit configurations are established by way of test results on a proto type.

Introduction

A common need arises for taking the ratio of two analog voltages, in many instrumentation and control applications. This operation is usually performed by a log-antilog network configuration [1]. An alternative method that has been proposed in the past is based on the FET [2],[3]. The fact that a FET can be used as a voltage dependent resistor, albeit within restricted gate-to-source voltage limits, is exploited in this method. Hence, this method is useful only for small voltage levels. A different approach that can be found in the literature [4] is to convert the input voltages to equivalent frequencies; take the ratio of two frequencies using conventional digital techniques; and then produce an output voltage proportional to the period this ratio-metric signal. This method is applicable only when the numerator voltage varies within a small specified range of values. S. I. Liu and J . J. Chen developed a scheme [5] in which the analog division was performed with two current feedback opamps, one resistor and two MOSFETs. N. I. Khachab and M. Ismail developed another scheme [6] by using one opamp and eight MOSFETs. Carlos A. De La Cruz Blas and Antonio Lopez developed a scheme [7] which is based on a CMOS translinear loop using a novel biasing scheme that allows class – AB operation. Munir A. Al – Absi proposed a circuit [8] which consists of four MOSFETs biased in weak inversion.

A square waveform is generated whose time period T is inversely proportional to one input voltage (V_1). Another input voltage (V_2) is integrated during the time period T. The peak value of the integrated output is proportional to the division V_2/V_1. This is called as double dual slope analog divider and is described in this paper. One dual slope integrator produces a triangular wave of time period T which is inversely proportional to the one input voltage V_1. The another dual slope integrator integrates the another input voltage V_2 during the period T and produces another triangular wave of peak value V_O which is proportional to the analog division V_2/V_1. The proposed analog divider has a better performance, even when the numerator voltage varies over a wide range.

Circuit Analysis

The circuit diagram of the proposed analog divider is shown in Fig. 1 and its associated waveforms in Fig. 2. A triangular wave is generated by alternatively charging and discharging a capacitor with a constant current. In Fig. 1 the triangular waveform is generated by the comparator OA3 and integrator OA2. The output of comparator OA3 is a square wave of amplitude approximately equal to ± Vcc and is applied to the transistor switch Q1. The output of OA2 is a triangular wave of peak value ± V_T and is fed back as input to the comparator OA3 through the voltage divider R_3 and R_4.

Let us assume initially output of comparator OA3 is at +Vcc, where ±Vcc is the power supply voltage to the circuit. This forces the transistor Q1 to ON and the non inverting terminal of the opamp OA1 to GROUND. Hence OA1 acts as an inverting amplifier and $+V_1$ is applied to the integrator OA2. A constant current $+V_1/R$ flow through capacitor C to give a negative going ramp at the output of the integrator OA2, as shown in Fig. 2. Therefore, one end of voltage divider is at a voltage +Vcc and the other end at the negative going ramp. When the negative going ramp reaches a certain value $–V_T$, the effective voltage at point 'P' becomes slightly below 0V.

As a result of the output of comparator OA3 switches from +Vcc to –Vcc. The transistor Q1 becomes OFF and the amplifier OA1 will work as non inverting amplifier. $–V_1$ is given to the integrator. This forces a reverse constant current through the capacitor C to give a positive going ramp at the output of integrator OA2 as shown in Fig. 2. When the positive going ramp reaches $+V_T$, the effective voltage at the point 'P' becomes slightly above 0V. As a result, the output of comparator OA3 switches from –Vcc to +Vcc. This sequence therefore repeats to give a triangular wave at the output of integrator OA2 and a square wave at the output of OA3.

When the comparator output is +Vcc and the input to the integrator is $+V_1$, the effective voltage at point 'P' is given by

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$$-V_T + \frac{R_3}{R_3 + R_4}[+V_{CC} - (-V_T)] \quad (1)$$

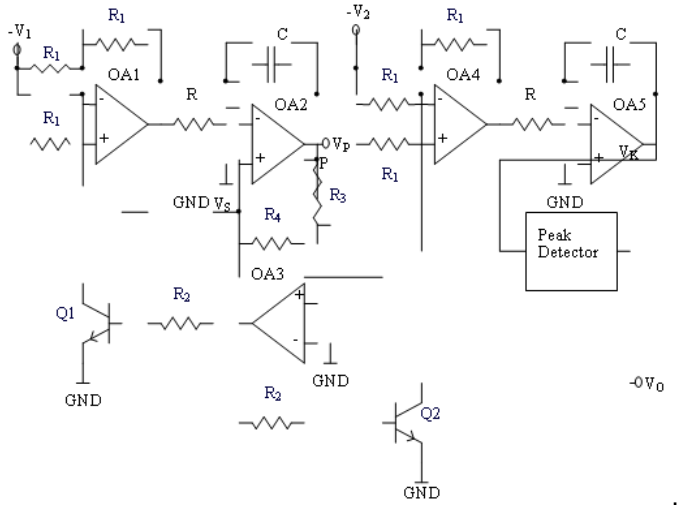

Fig. 1 Circuit diagram of double dual slope analog divider

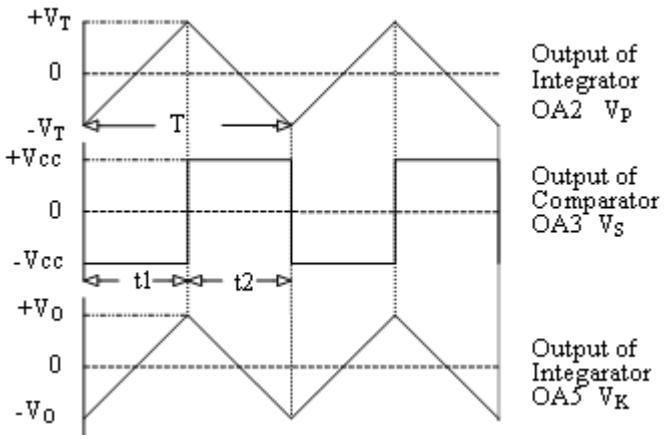

Fig.2 Associated waveforms of Fig. 1

When the effective voltage at P becomes to 0V, we can write the above equation as

$$-V_T + \frac{R_3}{R_3 + R_4}[+V_{CC} - (-V_T)] = 0 \quad (2)$$

From Eqn (2) we can get

$$-V_T = -\frac{R_3}{R_4}(+V_{CC}) \quad (3)$$

Similarly, when the comparator output is at –Vcc,

$$+V_T = \frac{R_3}{R_4}(-Vcc) \quad (4)$$

The integrator OA2 output V_P for one transition i.e when $+V_1$ is at its input will be

$$V_P(t) = -\frac{1}{RC}\int_0^t (+V_1)dt = -\frac{V_I}{RC}t_1 \quad (5)$$

From the waveform shown in Fig. 2 and the fact that at $t_1 = T/2$, $V_P(t) = 2V_T$, we get

$$2V_T = \frac{+V_1}{RC}\frac{T}{2} \quad (6)$$

$$T = \frac{V_T}{V_1}4RC \quad (7)$$

The Square wave form thus generated at the output of opamp OP3 is controlling the transistor switch Q2. During ON time of square wave, the transistor Q2 is ON and makes the opamp OA4 to work as inverting amplifier. $+V_2$ is given to the integrator OA5. Its output V_K will be

$$V_K(t) = \frac{1}{RC}\int_0^{T/2} -V_2 dt \quad (8)$$

$$V_K(t) = -\frac{V_2}{RC}t_1 \quad (9)$$

During OFF time of square wave, the transistor Q2 is OFF and makes the opamp OA4 to work as non inverting amplifier. $–V_2$ is given to the integrator OA5. Its output V_K will be

$$V_K(t) = \frac{1}{RC}\int_0^{T/2} V_2 dt \quad (10)$$

$$V_K(t) = \frac{V_2}{RC}t_2 \quad (11)$$

Another triangular wave with peak values ± V_O is generated at the output of the integrator OA5. From Fig. 2 and from the above equation, the fact that at $t_2 = T/2$, $VK(t) = 2V_0$

$$2V_O = \frac{V_2}{RC}\frac{T}{2} \quad (12)$$

$$V_0 = \frac{V_2}{V_1}V_T \quad (13)$$

$$V_O = \frac{V_2}{V_1}\frac{R_3}{R_4}(\pm Vcc) \quad (14)$$

The peak detector at the output of the integrator OA5 gives the peak value V_O.

Experimental Results And Conclusion

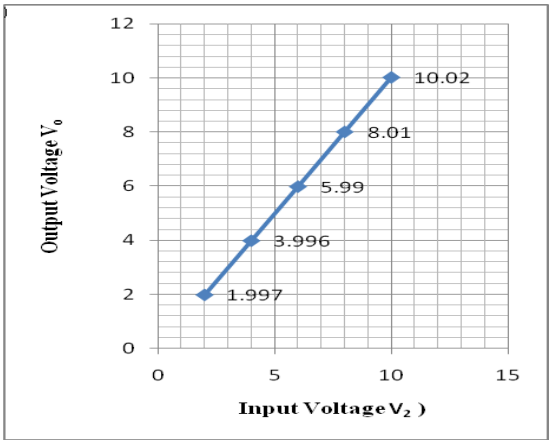

Fig. 3 Test results for ($-V_1$) = 9.1V

The proposed circuits were tested in our laboratory. LF 356 IC was used for all opamps. R_3 =10KΩ, R_4 = 15 KΩ, R = 47KΩ, C = 0.1μF, R_1 = R_2 = 1KΩ, were chosen. BC 547 transistor for Q1 and Q2 were used. ± 15 V power supply was given to the circuit. The practical ± Vcc was found to be ± 13.66V. One input voltage kept constant and another input voltage was varied and the test results are shown in the graphs of Figs.3-4. The offset in all opamps will cause an error in the result and hence it should be nulled. The input voltages V_1 and V_2 should only be

negative polarity. Hence the proposed divider is of single quadrant type.

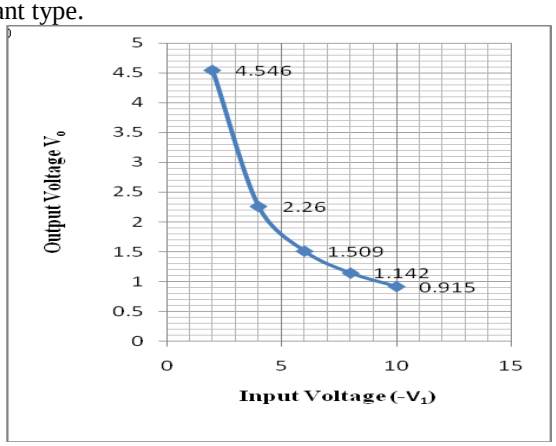

Fig. 4 Test results for (-V_2) = 1V

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