Available online at www.elixirpublishers.com (Elixir International Journal)

Electrical Engineering

Elixir Elec. Engg. 64 (2013) 19142-19145

ISSN: 2229-712X

Design and implementation of a nine level cascaded inverter for a PV system

R. Subha* and Rekha Radhakrishnan

Department of Electrical and Electronics Engineering, Sir M Visvesvaraya Institute of Technology, Bangalore.

ARTICLE INFO

Article history:

Received: 5 September 2013;

Received in revised form:

28 October 2013;

Accepted: 5 November 2013;

Keywords

Photovoltaic,

Multilevel inverter,

Selective harmonic elimination,

Total harmonic distortion.

ABSTRACT

In recent years energy generation from renewable sources in clean, efficient and environment friendly manner is a real challenge. Among the various non conventional sources, photovoltaic(PV) generation using multilevel inverter topologies are widely used due to the economy of use, flexibility in control under partially shaded conditions and the high quality of voltage waveforms. This work focuses on a single phase nine level cascaded inverter using PIC16F877A microcontroller to generate the required gate signals. The notch angles for the gate signals are calculated using selective harmonic elimination method. Using this method the total harmonic distortion is minimized by eliminating the most significant low frequency harmonic components from the voltage waveforms. The high frequency harmonic components can then be easily eliminated using additional filter circuits. The entire setup has been simulated in MATLAB and verified using the hardware setup.

Introduction

In the recent years there has been a significant increase in demand for electric power generation. However, the conventional generating systems, especially the thermo-electric power plants that use radioactive materials or fossil fuels have a significant environmental impact causing widespread pollution. Additionally, the cost of fossil fuel keeps increasing since the fossil fuel reserves are limited. Under these circumstances, alternative renewable energy source like solar, wind, geothermal, etc. has gained considerable attention. This combined with the new technological developments in renewable energy systems have made them commercially viable alternatives.

One of the major limitations of renewable energy systems is the lack of availability of constant and stable source of energy. In solar PV systems, sun irradiance might change quite a lot during the day. Therefore a stable grid interface is desired to filter the fluctuation in the renewable energy source to provide reliable power to the user. As such, most of the solar PV systems interface to the grid through a control circuitry. Solar PV cells provide DC voltage. The DC electric energy is converted into AC electric energy by using inverter. Inverters use power semiconductor devices whose output voltage is limited. Many different inverter circuit topologies are possible. Similarly, there are also numerous techniques available for the control of these inverters. Inverters can be operated in two or more levels of DC voltages depending on the circuit topology. Due to the numerous advantages over conventional two level inverters, multilevel inverters became very popular for the renewable energy systems in recent years. It is possible to run the power devices at lower frequencies using multilevel inverter topologies; the lower frequency operation yields better power conversion efficiency. Therefore multilevel inverter topologies are used to achieve higher power output voltage waveforms.

The control objective on the DC side is to capture maximum energy and deliver it to the utility grid. The energy captured by the system drives the system payback. Increasing the energy capture can have a substantial positive impact a more productive system is able to pay for itself more quickly.

Cascaded Multilevel Inverter Topology

A single-phase structure of an m-level cascaded multilevel inverter is depicted, where the individual PV panels or series-parallel connected portion of the PV panels are fed into single-phase H-bridge inverter modules. Each single-phase full-bridge inverter module generates three voltage levels at the output: $+V_{DC}$, 0 and $-V_{DC}$. The resulting phase voltage is obtained by the addition of the voltage generated by different inverter cells. This is made possible by connecting the DC voltage sources to the AC output by different combinations of the four power switches, S1, S2, S3 and S4. The number of output voltage levels, m in a cascaded inverter is defined by m = 2n+1, where n is the number of H-bridge inverter modules.

Fig 1 shows the bi-directional multilevel inverter topology for the solar PV arrays.

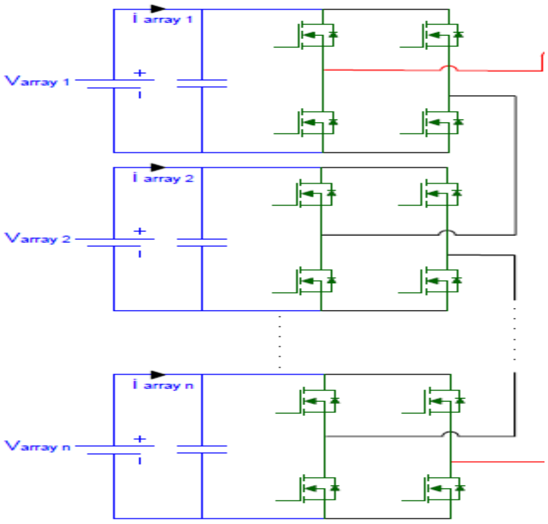

Figure 1. Bidirectional multilevel inverter topology

Tele:
E-mail addresses: subha.mvit@gmail.com

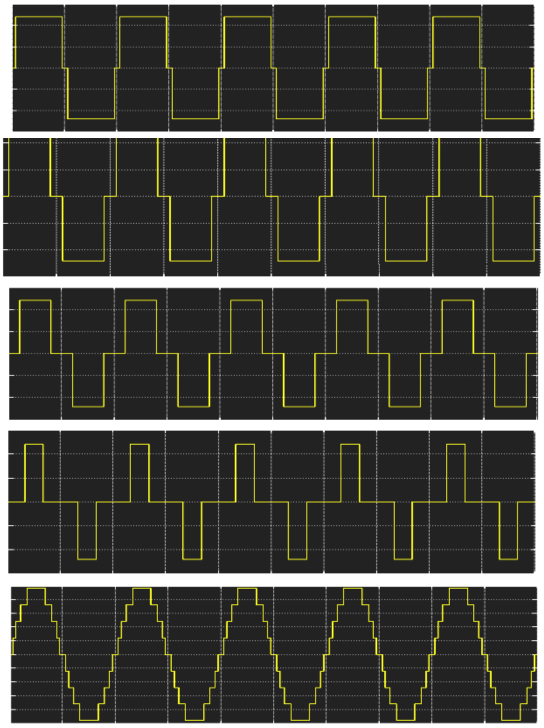

Figure 2. Output voltage of nine level inverter

The output voltage of the individual levels can be varied by varying the switching angles of the respective level switches. The switching angles must lie under the given range

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \frac{\pi}{2}$$

The selective harmonics elimination method is used to eliminate the 3rd, 5th and 7^{th} harmonics and switching angle calculation is made in that respect. Staircase voltage waveform is obtained which is much closer to sinusoidal waveform. Therefore, an effective reduction of total harmonics distortion is achieved.

Switching Angles

The switching angles are calculated using selective harmonic elimination method. Figure 3 shows a quarter-wave symmetric stepped voltage waveform synthesized by a (2m+1)-level inverter. The waveform has no even harmonics. The amplitude of any odd harmonic of this stepped-waveform can be expressed as follows:

$$h_n = \frac{4V_{dc}}{n\pi}[\cos(n\alpha_1) + \cos(n\alpha_2) + \dots\dots\dots + \cos(n\alpha_m)]$$

Where V_{dc} is the battery voltage and n is the odd harmonics angle

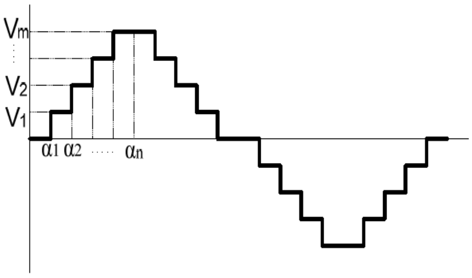

Figure 3. Generalized stepped voltage waveform

The switching angles are calculated by solving the following set of non-linear equations:

$$\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) = \pi$$

$$\cos(3\alpha_1) + \cos(3\alpha_2) + \cos(3\alpha_3) + \cos(3\alpha_4) = 0$$

$$\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \cos(5\alpha_4) = 0$$

$$\cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) + \cos(7\alpha_4) = 0$$

These non-linear equations were solved by writing a MATLAB program. The values of the switching angles obtained are as tabulated in Table 1.

Table 1: Switching Angles

Switching Angle	Angle in Radians
α_1	0.15
α_2	0.35
α_3	0.65
α_4	1.04

Hardware Implementation

The schematic block diagram of PV system and inverter is as shown below in figure 4. A 12 V solar panel is connected to each H-bridge circuit of a nine level inverter, through a charge controller and a battery. Gate pulses are given to the MOSFET from the PIC microcontroller. Isolator is used to give electrical isolation to either side of the system. Inverter converts the DC voltage from the solar panel to AC voltage. The output obtained from the inverter is the sum of all the four stages and amounts to 48 V.

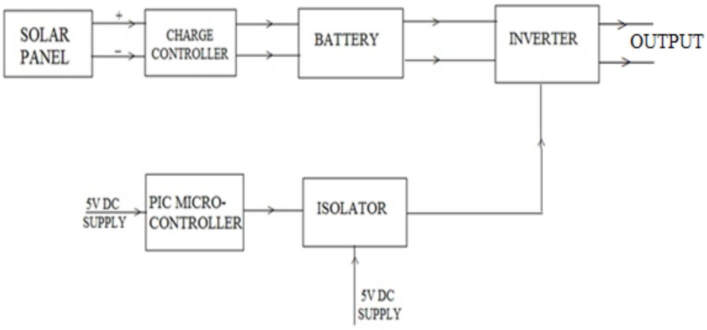

Figure 4. Schematic block diagram of PV system and inverter

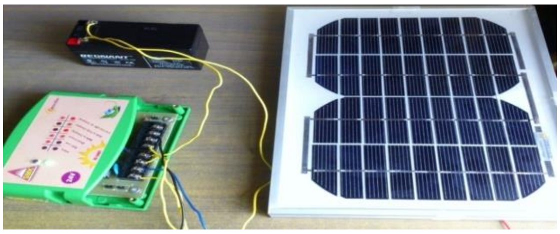

Figure 1. PV Module

Figure 2. Hardware implementation

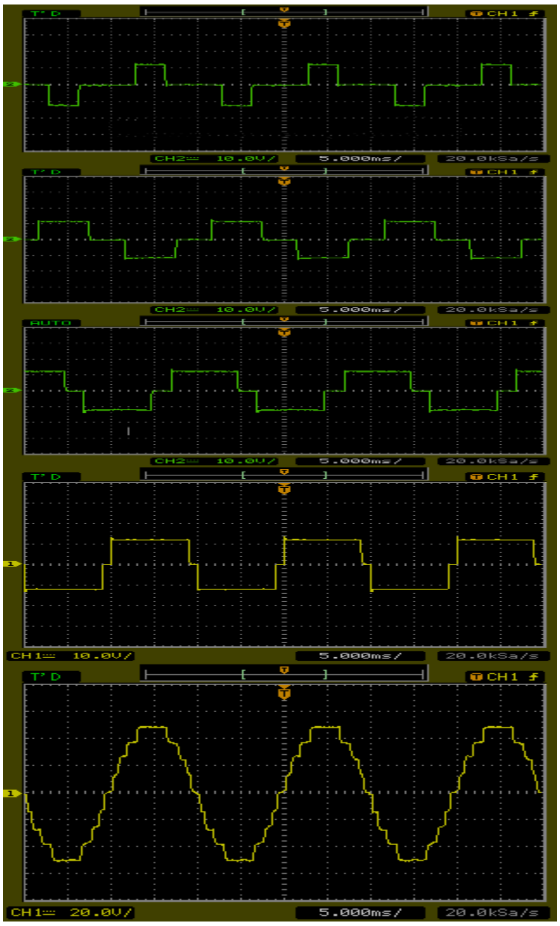

Figure 7. Hardware Results

The values obtained from the storage oscilloscope are used to write a program which shows the harmonics present in the output waveform**.**

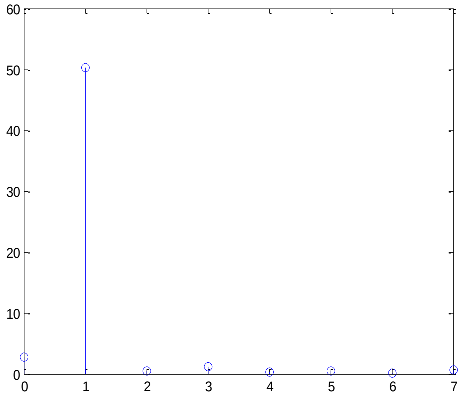

Figure 8. Harmonic spectra of output voltage

Figure 8 shows that the harmonic contents analysis of the output from the inverter do not contain, the 3rd, 5th and 7th harmonics. Hence selective harmonic elimination can be used to eliminate the third, fifth and seventh harmonics. The total harmonics distortion(THD) is reduced to 8.5%. Therefore, an effective reduction of total harmonics distortion is achieved.

Conclusion

A nine level cascaded inverter consisting of four H-bridges has been simulated in MATLAB. Selective harmonic elimination method is the pulse width modulation technique used to eliminate the required harmonics. The circuit has been designed for the elimination of 3rd, 5th and 7th harmonics and the switching angles are determined depending on the harmonics to be eliminated. The values of the switching angles thus calculated were found to be 9.1^{o}, 20.35^{o}, 37.3^{o} and 59.95^{o}. In the simulation results it is observed that the selected harmonics were eliminated successfully and the total harmonic distortion was 8.5%.

PIC microcontroller 16F877A was programmed to generate the gate pulses for the inverter circuit. The on and off time of the gate pulses depend on the values of the switching angles calculated. These gate pulses are given to the inverter circuit which consists of H-bridges constructed using MOSFETs IRFZ44. The output of the nine-level inverter thus obtained is analyzed to determine the harmonics present and the total harmonic distortion. It can be observed that the 3rd, 5th and 7th harmonics are not present in the output waveform and the total harmonic distortion is 8.5%.

Thus the results for the nine level cascaded inverter obtained from the simulation has been successfully validated using the hardware setup. This inverter has been powered using four 12V solar panels and gives an output voltage of around 50V. This inverter module can be extended for higher voltage applications by replacing the 12V solar panels by higher rated ones and can be thereby used for various domestic applications.

References

1. IEEE paper on *Energy Capture Improvement Of A Solar Pv System Using A Multilevel Inverter* by Nayeem Mahmud, Yilmaz Sozer, Iqbal Husain
2. International Journal of Engineering Science and Technology- *selective harmonics elimination of pwm cascaded multilevel inverter* by Aniket Anand, K.P.Singh
3. Kjaer, S.B., Pedersen, J.K., Blaabjerg, F., “A review of single-phase grid-connected inverters for photovoltaic modules,” *IEEE Transactions on Industry Applications*, vol. 41, no. 5, September/October 2005.
4. Sozer, Y., Torrey, D.A. , “Modeling and Control of Utility Interactive Inverters,”*IEEE Transactions on Power Electronics*, vol. 24, no. 11, November 2009.
5. Torrey, D.A., and Kokernak J. M., “Increasing the productivity of solar photovoltaic systems,” *Proceedings of American Solar Energy Society*, Solar 2006 Conference, July 8-13, 2006.
6. Mayer, D., Heidenreich, M., “Performance analysis of standalone PV systems from a rational use of energy point of view,” *Proceedings of 3rd World Conference on Photovoltaic Energy Conversion*, May 2003, pp. 2155-2158.
7. Gules, R., De Pellegrin Pacheco, J., Hey, H.L., Imhoff, J., “A Maximum Power Point Tracking System with Parallel Connection for PV Stand-Alone Applications,” *IEEE Transactions on Industrial Electronics*, Vol. 55, No 7, pp 2674-2683, Jul 2008.
8. Esram, T., Chapman, P.L., “Comparison of photovoltaic array maximum power point tracking techniques,” *IEEE Transactions on Energy Conversion*, vol. 22, no 2 pp. 439-449, June 2007.
9. Weidong Xiao, Ozog, N., Dunford, W.G., “Topology study of photovoltaic interface for maximum power point tracking,” *IEEE Transactions on Industrial Electronics*,vol. 54, no. 3, pp.1696-1704.
10. Jih-Sheng Lai, Fang Zheng Peng, “Multilevel converters – a new breed of power converters,” *IEEE Transactions on Industrial Applications*, vol. 32, pp. 509–517, October 1995.
11. Tolbert, L.M. Fang Zheng Peng Habetler, T.G., “Multilevel converters for large electric drives,” *IEEE Transactions on Industrial Applications*, vol. 35, pp. 36–44, January/February 1999.

12. R. Teodorescu, F. Beaabjerg, J. K. Pedersen, E. Cengelci, S. Sulistijo, B. Woo, and P. Enjeti, “Multilevel converters — A survey,” *Proceedings of European Power Electronics Conference*, Lausanne, Switzerland, 1999. 88

13. Rodriguez, J. Jih-Sheng Lai Fang Zheng Peng, “Multilevel Inverters: A Survey of Topologies, Controls and Applications,” *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, p p. 724-738, August 2002.

14. Nabae, Akira Takahashi, Isao Akagi, Hirofumi , “A new neutral-point clamped PWM inverter,” *IEEE Transactions on Industrial Electronics*, vol. IA-17, pp. 518–523, September/October 1981.

15. Meynard, T. A., Foch H., “Multi-level choppers for high voltage applications,” *European Power Electronic Drives Journal*, vol. 2, no. 1, p. 41, March 1992.

16. Hochgraf, C. Lasseter, R. Divan, D. Lipo, T.A., “Comparison of multilevel inverters for static var compensation,” *Industry Applications Society Annual Meeting*, pp. 921–928, October 1994.

17. Walker, G.R. Sernia, P.C., “Cascaded DC-DC Converter Connection of Photovoltaic Modules,” *IEEE Transactions on Power Electronics*, Vol. 19, No. 4, pp. 1130-1139, July 2004.

18. Linares, L. Erickson, R.W. MacAlpine, S. Brandemuehl, M., “Improved energy capture in series string photovoltaic via smart distributed power electronics” *IEEE Applied Power Electronics Conference and Exposition*, pp. 904-910, 2009.

19. Herrmann, W. Wiesner, W. Vaassen, W., “Hot spots investigations on PV modules—new concepts for a test standard and consequences for module design with respect to by-pass diodes”, *Proceedings of the IEEE Photovoltaic Specialists Conference*, pp. 1129–1132, 1997.

20. Klenk, M., Keller, S., Weber, L., Marckmann, C., Boueke, A., Nussbaumer, H., Fath, P., Burkhart, R., “Investigation of the hot-spot behavior and formation in crystalline silicon power cells, PV in Europe, from PV technology to energy solutions,” *Proceedings of the International Conference*, pp. 272–275, 2002.

21. Esram, T. Chapman, P.L., “Comparison of Photovoltaic Array Maximum Power Point Tracking Techniques”, *IEEE Transactions on Energy Conversion*, vol. 22, June 2007.

22. Quan Li Wolfs, P., “Recent Development in the Topologies for Photovoltaic Module Integrated Converters,” *Power Electronics Specialists Conference*, 2006.

23. Koizumi, H. Kurokawa, K., “A Novel Maximum Power Point Tracking Method for PV Module Integrated Converter” *IEEE Applied Power Electronics Conference and Exposition*, pp. 904-910, 2009.

24. H. Shan, Y. Kang, S. Duan, Y. Zhang, M. Yu, Y. Liu, G. Chen, F. Luo, “Research on novel parallel current sharing control technique of the stand-alone photovoltaic 89 inverter,” *Proceedings of the IEEE Annual Conference of the Industrial Electronics Society*, pp. 1645-1649, November 2007.

25. Khan, I.A. , “Battery Chargers For Electric And Hybrid Vehicles”, *IEEE Transaction on Power Electronics in Transportation*, October 1994.

26. Sirisukprasert, S. Jih-Sheng Lai Tian-Hua Liu, “Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters,” *IEEE Industry Applications Conference*, pp. 2094–2099, October 2000.

27. Muyulema, S. Bueno, E.J. Rodriguez, F.J. Cobreces, S. Diaz, D., “Response of the grid converters synchronization using P. U. magnitude in the control loop,” *IEEE International Symposium on Industrial Electronics*, pp. 186–191, June 2007.

28. Freijedo, F.D. Doval-Gandoy, J. Lopez, O. Cabaleiro, J., “Robust phase locked loops optimized for DSP implementation in power quality applications,” *Annual Conference of IEEE Industrial Electronics*, pp. 3052–3057, November 2008.

29. Camargo, R. F., Pinheiro, H., “Synchronization method for three phase PWM converters under unbalanced and distorted grid,” *Power Electronics Specialists Conference*, vol. 153, no. 5, pp. 763–772, September 2006.

30. Guan-Chyun Hsieh Hung, J.C., “Phase-locked loop techniques: A survey,” *IEEETransactions on Industrial Electronics*, vol. 43, no. 6, pp. 609–615, December 1996.

31. Iwase Hisashi, I. Osamu, T. Katsuya, “WT3000 Precision Power Analyzer, ”*Yokogawa Technical Report English Edition*, no. 39. 2005.