



# A Novel Nanometric Efficient Reversible Low Power Parity Preserving Full Adder/Subtractor

Ali Bolhassani<sup>1</sup>, Mahdiar Ghadiry<sup>1</sup>, Soudabeh Boroumand<sup>2,\*</sup> and Nayereh Hosseininia<sup>2</sup>

<sup>1</sup>Department of Computer Engineering, Arak Branch, Islamic Azad University, Arak, Iran.

<sup>2</sup>Young Researchers and Elite Club, Tabriz Branch, Islamic Azad University, Tabriz, Iran.

## ARTICLE INFO

### Article history:

Received: 9 September 2013;

Received in revised form:

19 December 2013;

Accepted: 20 January 2014;

### Keywords

Reversible parity preserving full adder/subtractor,  
Parallel adder/subtractor,  
Carry skip adder/subtractor,  
VHDL.

## ABSTRACT

In this paper, a new 5×5 reversible parity preserving gate is proposed and employed to realize 1-bit reversible parity preserving full adder/subtractor. The proposed 1-bit full adder/subtractor is implemented using VHDL and compared to previously presented designs in the literature. The results show that the proposed design is more efficient in terms of number of DC inputs/outputs, delay and quantum cost. Also two reversible parity preserving four-bit parallel adder/subtractor and carry skip adder/subtractor are designed applying the proposed scheme and compared to the former designs.

© 2014 Elixir All rights reserved

## Introduction

Consistent with increasing advances in various sciences, high speed computers are required. Designers of the integrated circuits have tried to draw more functional circuits to increase computers' processing power. In 1965, Moore pointed out a theory to predict the computers' hardware development in coming years that is termed Moore's law [1]. According to this law, computers' power will roughly double every two years; but one of the major problems in very large scalable integrated circuits design is the elimination of thermal energy which is created by circuit transistors. Low power circuit design with increasing portable electronic devices such as cell phones and handheld computers has become a major issue for designers of the digital circuits.

Information loss which causes energy to dissipate is not ignorable in Nano-scale technologies, which are the technology of the future designs. In 1961, Landauer [2] showed that if a circuit performs data processing on an irreversible trend,  $kT \ln 2$  joules of heat energy will generate, where  $k$  is Boltzmann's constant and  $T$  is the absolute temperature at which computation is performed. This energy loss was much lower than static and dynamic energy of a transistor; but in future this won't be insignificant. In 1973, Bennett [3] proved that if the circuit included reversible gates, energy loss would not occur.

In reversible logic, every input pattern has a unit output pattern. Thus, the number of inputs and outputs in reversible circuits is the same. Designing reversible circuits by reversible gates has two restrictions [4]:

- Each signal has one fan out.
- Feedback is not allowed.

Reversible parity preserving full adder/subtractor is an important circuit in digital designs. Full adder is one of the most important blocks of large circuits such as 32-bit adders and multipliers. In addition, using parity circuit in full adder makes the circuit fault tolerant. Therefore, any improvement in this design will result in significant improvement of the whole

system. According to our literature review, there is a lack of research in this area. As a result, we were motivated to improve the current works in [5-7]. In this paper, a new reversible parity preserving full adder/subtractor is presented which is optimized in terms of gates count, number of constant inputs, number of garbage outputs, delay and quantum cost.

## Previous work

Parminder Kaur & Balwinder Singh Dhaliwal in [5] presented a paper on design of fault tolerant full adder/subtractor using reversible gates. Firstly they suggested fault tolerant half adder then designed a reversible fault tolerant full adder/subtractor by combination of two reversible fault tolerant half adder/subtractor (FTHA\_S) blocks and one F2G. They used VHSIC for simulation.

Prashanth.N.G and et al in [6] suggested a more efficient fault tolerant full adder/subtractor with MIG than Parminder's paper. They made a reversible FT\_FA/S\_P block with less QC, garbage outputs, constant inputs and number of gates. Then they extended the design to fault tolerant parallel adder/subtractor and fault tolerant carry skip adder/subtractor. Another reversible optimized fault tolerant full adder/subtractor was presented by Prashanth. N.G with et al in [7]. They improved the design proposed in [5] in terms of evaluated parameters. According to the results reported in [7], the number of gates, constant inputs and garbage outputs are reduced 44.45 and 36.36 percentages respectively.

## The proposed design

In this section, first a block named BBFS is presented, which is later is used as the basic block the full adder/subtractor. Second parity preserving parallel adder/subtractor and carry skip adder/subtractor is offered.

## New reversible parity preserving BBFS gate

The block diagram of the proposed reversible parity preserving BBFS gate is shown in fig.1. Reversible parity preserving BBFS is a 5×5 gate with inputs (A, B, C, D, E) and outputs (P, Q, R, S, T). It is a universal gate i.e. any logical

reversible circuit can be created using this gate. The implementation of the proposed gate by elementary quantum gates is depicted in fig.2. Two V-boxes are used to denote a controlled-V gate and one V<sup>+</sup>-box is used to denote a controlled-V<sup>+</sup> gate. The quantum realization of BBFS requires one dotted rectangles, one V, one V<sup>+</sup> and nine Feynman gates. Dotted rectangle is equivalent to a Feynman gate with QC=1. So the total QC equals 12.

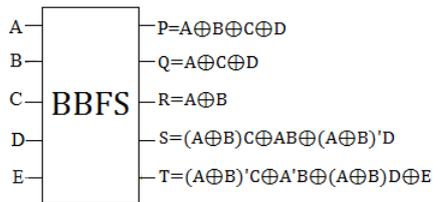


Fig. 1. The block diagram of proposed reversible parity preserving BBFS gate

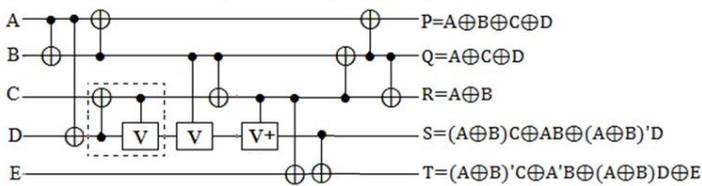


Fig. 2. Quantum realization of the proposed reversible parity preserving BBFS gate

**New reversible parity preserving full adder/subtractor**

The proposed circuit illustrated in fig.3 is realized using BBFS and FRG gates. The proposed circuit has 6 inputs consisting of A, B, C inputs, Ctrl signal using as control of operation and two constant inputs. If Ctrl signal is set to zero then the circuit works as a reversible parity preserving full adder else it will operate as a reversible parity preserving full subtractor. The block diagram of the proposed reversible fault tolerant full adder/subtractor (FTFA/S) has demonstrated in fig.4. Proposed design has 2 main outputs consisting S/D and C/B lines which are sum/difference and carry/Borrow outputs respectively, a P=A ⊕ B output which is used in designing carry skip adder/subtractor and also has 3 garbage outputs with QC=17. Quantum cost, garbage outputs, constant inputs, delay and gate counts are six parameters for determining the complexity and performance of reversible circuits [8, 9]. Optimization of these parameters is very crucial in the design of reversible circuits. So we proposed a new full adder/subtractor which has lowest QC and delay compared to previous designs. In addition, the proposed circuit has less number of garbage outputs which is resulted higher performance.

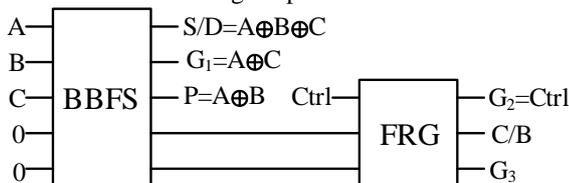


Fig. 3. The proposed parity preserving reversible full adder/subtractor circuit(FTFA/S)

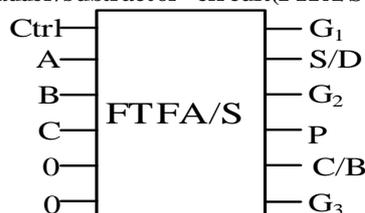


Fig. 4. Block diagram of the proposed reversible fault tolerant full adder/subtractor(FTFA/S)

**New reversible parity preserving 4-bit parallel adder/subtractor**

A parity preserving 4-bit parallel adder/subtractor consisting of proposed FTFA/S block is depicted in fig.5. It constructed by cascading 4 number of reversible parity preserving full adder/subtractor blocks. In a parallel arithmetic unit, all 8 input bits are usually available to the adder/subtractor at the same time. However, the carries have to propagate from the FTFA/S block in position 0 to position 3 to produce the correct sum/difference and carry/Borrow bits. The mode of operations is controlled by Ctrl signal. If Ctrl=0, entered 4-bit operands will be added simultaneously and if Ctrl=1 the inputs will be subtracted.

**New reversible parity preserving 4-bit carry skip adder/subtractor**

The parallel adder describing in 3.3 section is called ripple carry adder because every S/D output of FTFA/S block needs to wait for the carry-in from the previous FTFA/S cell, so it is simplest adder but has the longest delay for propagating carry. An n-bit parallel adder has a delay of O(n) while the carry skip adder has a delay of O(√n). The needed time for propagating the carry is reduced by skipping over groups of sequential adder/subtractor stages in carry skip adder/subtractor. In other words, in carry skip adder/subtractor every FTFA/S stage can be bounced if inputs a<sub>i</sub> ≠ b<sub>i</sub> it means if a<sub>i</sub> ⊕ b<sub>i</sub> = 0 the inputs will be identical and carry may be generate otherwise the inputs will be different and the carry/borrow input will propagate to carry/borrow output without waiting for rippling. For example a particular group of FTFA/S blocks consisting k bit positions 0,1,...,k-1, with C/B<sub>in</sub> signal as input carry/Borrow create the carry/Borrow out for group based on (1).

$$\frac{C}{B}_{out\ of\ group} = C_k + P_i \cdot \frac{C}{B}_{in} \cdot P_i = a_i \oplus b_j \tag{1}$$

So in carry skip adder/subtractor if P<sub>i</sub> of group is set to one then several consecutive stages can be skipped. Otherwise C<sub>k</sub> is selected which is allowed to propagate through all the remaining bit positions in group. Fig.6 depicts a parity preserving 4-bit carry skip adder/subtractor consisting of two groups each of size 2. The signals P<sub>0:1</sub> for first group and P<sub>2:3</sub> for second group can be generated simultaneously allowing a fast skip of groups which satisfy P<sub>0:1</sub>=1 and P<sub>2:3</sub>=1. In other words, if ctrl input in FRG was zero then the carry will propagate from first cell to last cell otherwise if Ctrl input sets one then the carry/Borrow-in will propagate directly to carry/Borrow out.

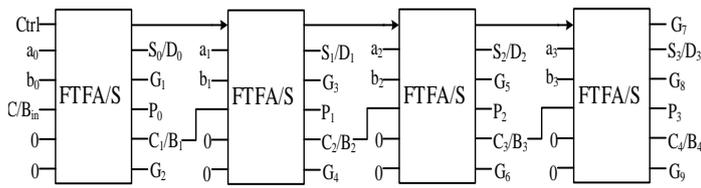
**Analytical analysis**

This section offers the necessary formulas for evaluation of n-bit parallel adder/subtractor as presented here. With these formulas, it is needless to draw complicated and time-consuming figures for computing the parameters of the reversible proposed circuits and we can calculate necessary parameters for any arbitrary number of bits. Let N<sub>FTFA/S</sub> be the total number of Full adder/subtractor block, GO, CON, QC be the total number of DC outputs/inputs and quantum cost of proposed design respectively, then:

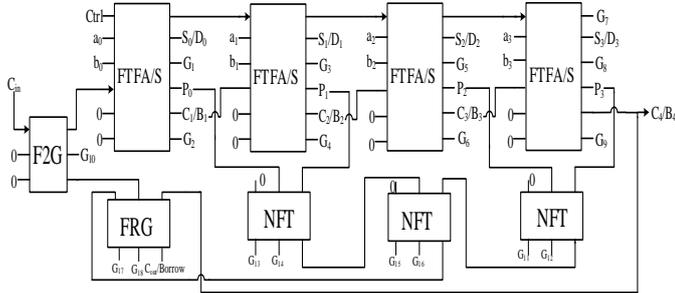
$$\begin{aligned} N_{FTFA/S} &= n \\ GO &= 2n + 1 \\ CON &= 2n \\ QC &= 17n \end{aligned}$$

**Proof.** adder/subtractor circuit has two n-bit inputs and every two bits requires one full adder/subtractor thus for adding or subtracting two n-bit numbers n blocks of FTFA/S is required and every block is consisting of two BBFS and FRG gates so the

total number of gates for constructing parallel adder/subtractor is  $2n$ .



**Fig. 5. The proposed parity preserving 4-bit parallel adder/subtractor circuit (ripple carry adder/subtractor)**



**Fig. 6. The proposed parity preserving 4-bit carry skip adder/subtractor circuit**

In adder/subtractor circuit every FTFA/S block produces 2 garbage outputs except last one has 3 garbage outputs. So the circuit begets  $2n+1$  garbage outputs. As well as every FTFA/S block produces 2 constant inputs which is  $2n$  DC inputs. One most common comparison criterions of quantum and reversible circuits is calculating the quantum cost of proposed circuit. The proposed parity preserving  $n$ -bit parallel adder/subtractor realized by  $n$  FTFA/S blocks and the quantum cost of every block is 17. Thus the total cost of proposed design is  $17 \times n$ .

The essential formulas for assessment of  $n$ -bit carry skip adder/subtractor are presented as follows. Let  $N_{FTFA/S}$ ,  $N_{F2G}$ ,  $N_{NFT}$  and  $N_{FRG}$  be the total number of Full adder/subtractor block, Feynman double gate, New fault tolerant gate and Fredkin gate respectively, GO, CON be the total number of DC outputs and inputs respectively, QC be the total number of quantum cost of proposed design, then

$$N_{FTFA/S} = n$$

$$N_{F2G} = 1$$

$$N_{FRG} = 1$$

$$N_{NFT} = n - 1$$

$$GO = 4n + 2$$

$$CON = 3n + 1$$

$$QC = 22n + 2$$

**Proof.** Carry skip adder/subtractor circuit has two  $n$ -bit inputs and every two bits requires one full adder/subtractor thus for adding or subtracting two  $n$ -bit numbers  $n$  blocks of FTFA/S is required and every block is consisting of two BBFS and FRG gates. Fan-out gates are exerted for copying signal in reversible circuit. One of the fan-out gates with parity preserving feature is F2G. The  $n$ -bit carry skip adder/subtractor requires one F2G for duplicating carry/Borrow input ( $C/B_{in}$ ). The forth output of reversible parity preserving full adder/subtractor block is  $P = A \oplus B$ . In proposed reversible parity preserving carry skip adder/subtractor if equation  $P = P_0 \cdot P_1 \cdot P_2 \cdot P_3$  sets one then carry/Borrow input directly propagate to carry/Borrow output. NFT gates are applied as AND gates to obtain the value of P signal so every  $n$ -bit carry skip adder/subtractor needs  $n-1$  NFT gates. As well as if the value in P signal was zero the carry output must be calculated by cascading full adder/subtractor blocks. So every  $n$ -bit carry skip adder requires one Fredkin gate

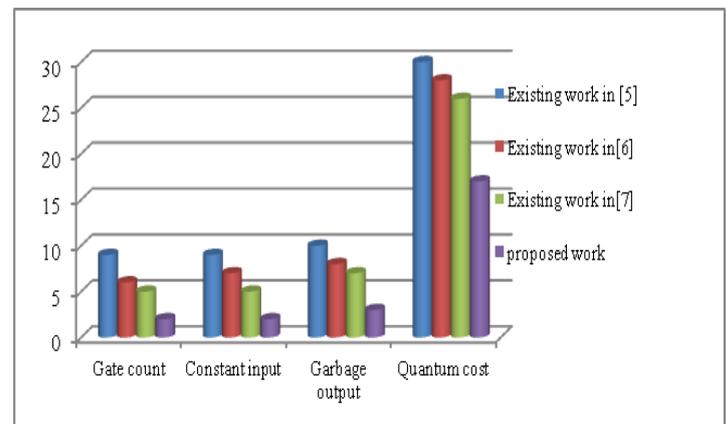
with P control signal. It means that depending on the value of P,  $C/B_4$  signal or  $C/B_{in}$  passes to the third output of Fredkin gate. In Adder/subtractor every NFT, FRG and FTFA/S gate produces 2 garbage outputs except the last FTFA/S block that generates 3 garbage outputs. F2G also create one garbage output so the  $n$ -bit carry skip adder will have a total of  $4n+2$  DC outputs. As well as F2G and every FTFA/S block needs 2 constant inputs which is  $2n+2$ . Every NFT gate has one DC input which is  $n-1$ . So the number of constant inputs equals  $3n+1$ . The proposed circuit is realized by NFT, F2G, FRG gates and FTFA/S block with quantum costs 5, 2, 5 and 17 respectively. Thus the total cost of proposed design is  $QC = 5N_{FRG} + 2N_{F2G} + 5N_{NFT} + 17N_{FTFA/S}$ .

**Simulation results**

The presented reversible parity preserving full adder/subtractor has three major advantages. First, it produces lowest quantum cost than the previous designs. Second, the worst-case delay for proposed circuit is significantly lower, since the quantum cost of the longest path from input to output is low. The third advantages is the number of garbage outputs playing an important role in evaluation of reversible circuits and a reversible is more optimized than other if have less garbage outputs. Table 1 shows the comparison of proposed parity preserving full adder/subtractor with other designed circuits in [5-7]. The comparative results in the form of graphical are also represented in fig.7.

**Table 1. Comparative Results of Different Reversible Parity Preserving Full Adder/Subtractor Circuits**

Design	Operations	Gate Count	Constant Inputs	Garbage Output	Quantum Cost	Delay
This Work	PP-FA/S-P*	2	2	3	17	9
Existing Design [7]	PP-FA/S	5	5	7	26	14
Existing Design [6]	PP-FA/S-P	6	7	8	28	16
Existing Design [5]	PP-FA/S	9	9	10	30	18

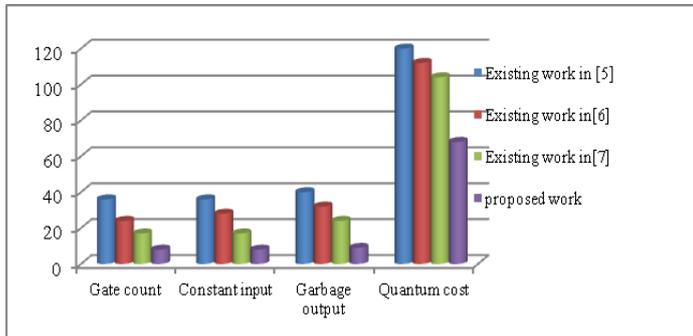


**Fig. 7. The Graphical Comparison of Different Fault Tolerant Full Adder/Subtractor**

We compare the proposed parity preserving 4-bit parallel and carry skip adder/subtractor with other previous designs in table 2 and 3 and fig.8 and fig.9. According to the obtained results the proposed parity preserving parallel adder/subtractor is composed of 8 gates, 9 garbage outputs, 8 constant inputs with  $QC=68$  and  $delay=36$ . As well as the proposed parity preserving carry skip adder/subtractor is composed of 13 gates, 18 garbage outputs, 13 constant inputs with  $QC=90$  which are less in comparison of proposed pervious circuits.

**Table 2. Comparative Results of Different Reversible 4-Bit Parity Preserving Ripple Carry Adder/Subtractor**

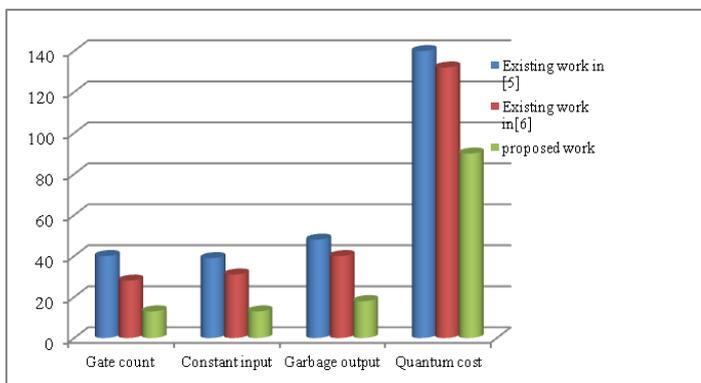
Design	Operations	Gate Count	Constant Inputs	Garbage Output	Quantum Cost	Delay
This Work	PP-FA/S-P*	8	8	9	68	36
Existing Design [7]	PP-FA/S	17	17	24	104	52
Existing Design [6]	PP-FA/S-P	24	28	32	112	60
Existing Design [5]	PP-FA/S	36	36	40	120	68



**Fig. 8. The Graphical Comparison of Different Fault Tolerant 4-bit Parallel Adder/Subtractor**

**Table 3. Comparative Results of Different Reversible 4-Bit Parity Preserving Carry Skip Adder/Subtractor**

Design	Operations	Gate Count	Constant Inputs	Garbage Output	Quantum Cost	Delay
This Work	PP-FA/S-P*	13	13	18	90	56
Existing Design [6]	PP-FA/S-P	28	31	40	132	80
Existing Design [5]	PP-FA/S	40	39	48	140	88



**Fig. 9. The Graphical Comparison of Different Fault Tolerant 4-bit Carry Skip Adder/Subtractor**

**Conclusions**

This paper proposed a reversible optimized parity preserving full adder/subtractor which is the combination of BBFS and FRG gates. This circuit was used in implementation of parity preserving parallel adder/subtractor and Carry Skip Adder/Subtractor. The proposed circuits have been implemented using VHDL code and simulated using Quartus Simulator. The proposed designs were evaluated in terms of the number of gates, number of garbage outputs, number of constant inputs, quantum cost and delay. The reported results indicated the superiority of the proposed designs compared to previous circuits. In addition, we proposed analytical analysis of the proposed circuit to show their efficiency for n bits.

**References**

- [1] G. E. Moore. Cramping more components onto integrated circuits. *Journal of Electronics*, 1965, 38: 114-117.
- [2] R. Landauer. Irreversibility and heat generation in the computing process. *IBM J. Res. Develop*, 1961, 5(3): 183-191.
- [3] C. Bennett. Logical reversibility of computation. *IBM J. Res. Develop*, 1973, 17(6):525-532.
- [4] H. M. H. Babu, M. R. Islam, A. R. Chowdhury, Syed Mostahed Ali chowdhury. Reversible Logic Synthesis for Minimization of Full-adder circuit. *IEEE Conference on Digital System Design, Euro-Micro '03, BeleK, Antalya, Turkey*, 2003:50-54.
- [5] Parminder Kaur, Balwinder Singh Dhaliwal. Design of Fault Tolerant Full Adder/Subtractor Using Reversible Gates. *International conference on computer Communication and Informatics (ICCCI-2012)*, Jan, 2012:10-12, Combatore, INDIA 978-1-4577-1583-9/12/\$26.00 © 2012 IEEE.
- [6] N.G. Prashanth, S.B. Manojkumar, B.S. Balaji, G. Naveena Pai and V.B. Havyas. Design and Synthesis of Reversible Fault Tolerant Carry Skip Adder/Subtractor. *International Journal of Emerging and Engineering (IJESE)*. June 2013, 8(1).
- [7] N.G. Prashanth, A.P. Savitha, M.B. Anandaraju, A.C. Nuthan. Design and Synthesis of Fault Tolerant Full Adder/Subtractor Using Reversible Gates. *International Journal of Engineering Research and Applications(IJERA)*, Jul-Agu 2013 4(3):137-142.
- [8] M.S. Islam, M.M. Rahman, Z. Begum and M.Z. Hafiz. Low cost quantum realization of reversible multiplier circuit. *Information Technology Journal*, 2009, 8(2):208-213.
- [9] F. Naderpour, A. Vafaei. Reversible multipliers: Decreasing the depth of the circuit. *Proceedings of 5<sup>th</sup> international conference on Electrical and Computer Engineering, Bangladesh*, 2008:306-310.