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Realization of S-G Shapers for Detector Readout Front Ends

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ABSTRACT

This paper presents realization of semi Gaussian (S-G) shaper circuits for detector readout front ends. The circuits are based on current difference transconductance amplifier (CDTA) and differential difference current conveyor transconductance amplifier (DDCCTA) and can operate in voltage and current mode. The proposed circuits use grounded capacitors and thus make these suitable from integration viewpoint. The theoretical propositions are verified through extensive SPICE simulations using 0.25µm TSMC CMOS technology model parameters. The performance of proposed topologies is compared in terms of total harmonic distortion, power dissipation, dynamic range, signal to noise ratio (SNR) and output noise. The performance comparison of CDTA, DDCCTA, CCII and OTA based shapers proves that proposed CDTA and DDCCTA based shapers have advantageous performance features over existing CCII and OTA based shapers.

Introduction

Recently, there is a considerable interest in developing monolithic implementation of readout systems [1]-[11]. The architecture of readout system comprises of a preamplifier stage followed by a pulse shaper [12]-[18]. The design of pulse shapers in integrated circuits is challenging as realization of long shaping times require resistances and capacitors of large values, thereby occupy a large implementation area. It is suggested that a semi Gaussian (S-G) shaper provides optimum signal to noise characteristics among other pulse shaping schemes [5], [19], [20]. The S-G shapers have primarily been implemented using *RL-RC*^{n} filter [19],[20] which is shown in Fig. 1. The S-G shaper is characterized by a lower and an upper frequency bound and can be seen as $(n+1)^{th}$ order band pass filter (BPF), where n represents number of lossy integrators. The transfer function of an nth order S-G shaper may be written by (1).

$$T(s) = \left(\frac{s\tau_{diff}}{1+s\tau_{diff}}\right)\left(\frac{A}{1+s\tau_{\text{int}}}\right)^n \quad (1)$$

where n is shaper order, τ_{diff} and τ_{int} are differentiator and integrator time constants, and A is integrators dc gain. The differentiator sets the pulse duration by introducing the decay time constant whereas the integrator increases rise time to limit noise bandwidth. The operating bandwidth of an S-G shaper may be computed by (2).

$$BW = f_{\text{int}} - f_{diff} = \frac{1}{2\pi\tau_{\text{int}}} - \frac{1}{2\pi\tau_{diff}} \quad (2)$$

The analog integrated circuits design, in particular S-G shaper, using current mode building blocks has gained popularity due to advantageous performance features like wide bandwidth, wide dynamic range, low power consumption, less circuit complexity, and high operating speed [20]. The literature survey on S-G shaper circuits shows that a variety of current mode active building blocks (ABB) namely operational transconductance amplifier (OTA) [20], second generation current conveyor (CCII) [20] and Current amplifiers (CA) [5] have been employed in the realization. In this paper, voltage and current mode S-G shaper designs based on current difference transconductance amplifier (CDTA) [21]-[24] and differential difference current conveyor transconductance amplifier (DDCCTA) [25]-[27] have been proposed. The proposed shaper configurations employ lesser passive elements and have better performance characteristics than the configurations described in [28]-[29]. The feasibility of the proposed designs is studied using SPICE simulations and their performance is compared in terms of total harmonic distortion (THD), power dissipation, and dynamic range (DR), signal to noise ratio (SNR) and output noise.

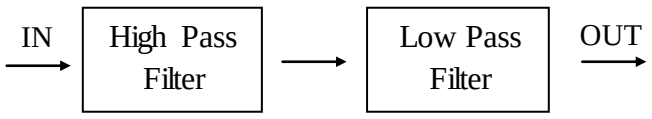

Fig 1. Block diagram of nth order S-G shaper

CDTA based shapers

CDTA [21]-[24] is an active and versatile circuit element which is free from parasitic input capacitances and can operate in a wide frequency range due to its current-mode operation. It consists of a unity-gain current source controlled by the difference of the input currents and a multi-output transconductance amplifier providing electronic tunability through its transconductance gain. The CDTA symbol is shown in Fig. 2 and its terminal characteristic in matrix form are given by (3).

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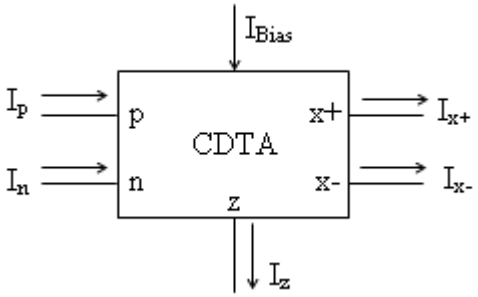

Fig 2. Symbol of CDTA

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ V_X \\ I_Z \\ I_{O1-} \\ I_{O2-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -g_m & 0 & 0 \\ 0 & 0 & 0 & 0 & -g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ V_Z \\ V_{O1-} \\ V_{O2-} \end{bmatrix} \quad (3)$$

where $g_m$is transconductance of the CDTA. The CMOS implementation of CDTA [22] is given in Fig. 3. It comprises of a current differencer (Mc1–Mc17) [22] which is followed by transconductance amplifier (Mc18–Mc26). The value of transconductance (g_m)is expressed by (4) which can be adjusted by bias current I_{Bias} of CDTA. transconductance (g_m)is expressed by (4) which can be adjusted by bias current $I_{Bias}$of CDTA.

$$g_m = \sqrt{2\mu C_{ox}(W/L)_{19,21} I_{Bias}} \quad (4)$$

where μ represents the carrier mobility, $(W/L)_i$is the aspect ratio of i^{th}transistor and $C_{ox}$is the gate oxide capacitance per unit area. The CDTA based voltage and current mode shaper circuits are proposed respectively in the next section.

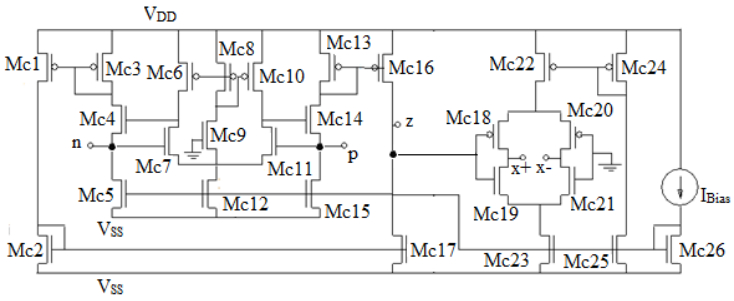

Fig 3. CMOS implementation of CDTA

CDTA based voltage mode shaper

The proposed voltage mode n^{th} order CDTA based S-G shaper circuit is shown in Fig. 4. It employs *(n+1)* CDTAs, two TAs, *(n+1)* grounded capacitors and two grounded resistors. The differentiator employs one CDTA, twoTAs, one grounded capacitor and resistor while *n* integrators employ *n* CDTAs, *n* grounded capacitors and onegrounded resistor. The transfer function of the proposed n^{th} order shaper and its operating bandwidth is given by (5) and (6) respectively.

$$T(s)_{VM\_CDTA} = (-1)^{n+1}\left(\frac{s\frac{g_1C_1}{g_3g_4R_1}}{1+s\frac{g_1C_1}{g_3g_4}}\right)\left(\frac{\sqrt[n]{R_2}}{1+s\frac{C_2}{g_2}}\right)^n \quad (5)$$

$$BW_{VM\_CDTA} = f_{int} - f_{diff} = \frac{1}{2\pi}\left(\frac{g_1g_2C_1 - g_3g_4C_2}{g_1C_1C_2}\right) \quad (6)$$

CDTA based current mode shaper

Fig. 5 shows the proposed n^{th} order CDTA based current mode shaper circuit. The circuit employs *(n+1)* CDTAs, two TAs and *(n+1)* grounded capacitors. The differentiator employs

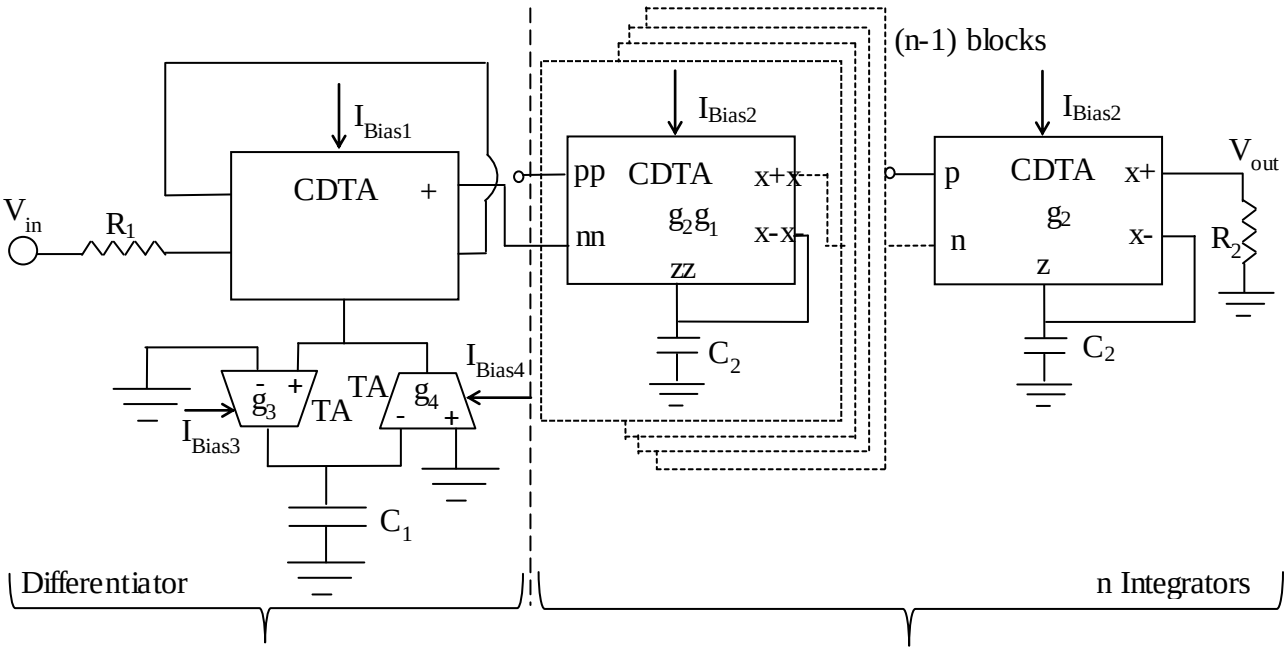

Fig 4. Proposed voltage mode n^{th} order CDTA based S-G shaper

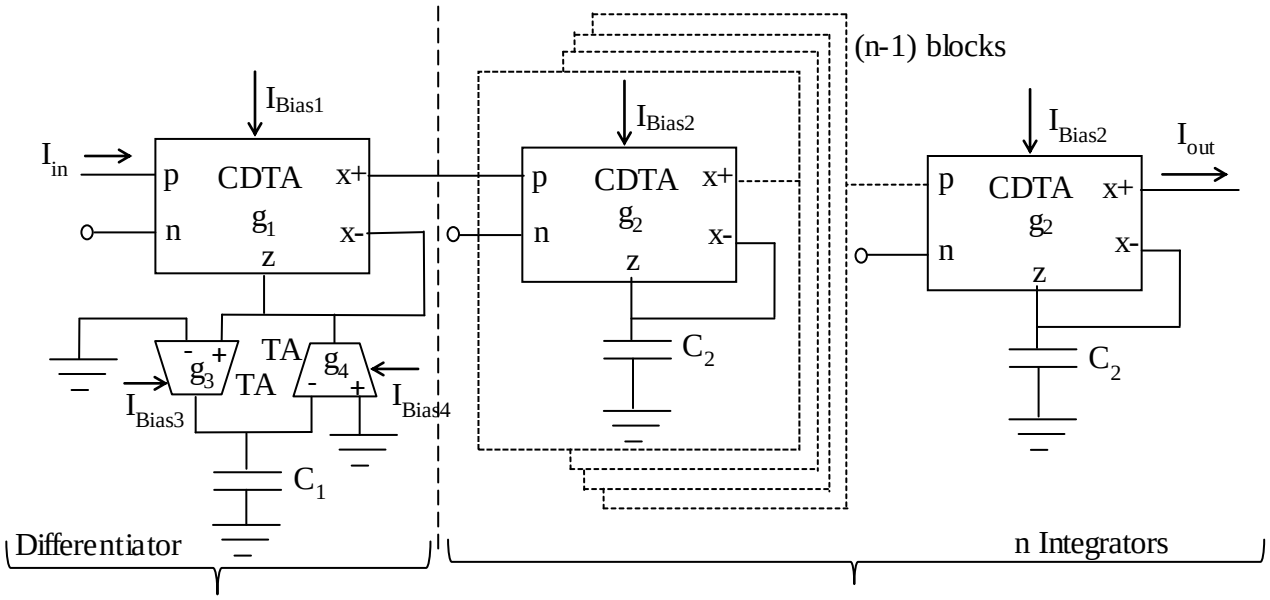

Fig 5. Proposed current mode n[th] order CDTA based S-G shaper

one CDTA, two TAs and one grounded capacitor while *n* integrators employ *n* CDTAs and *n* grounded capacitors. The transfer function of the proposed n^{th} order current mode shaper and its operating bandwidth is given by (7) and (8) respectively.

$$T(s)_{CM\_CDTA} = \left(\frac{s\frac{g_1 C_1}{g_3 g_4}}{1+s\frac{g_1 C_1}{g_3 g_4}} \right) \left(\frac{1}{1+s\frac{C_2}{g_2}} \right)^n \tag{7}$$

$$BW_{CM\_CDTA} = f_{\text{int}} - f_{diff} = \frac{1}{2\pi}\left(\frac{g_1 g_2 C_1 - g_3 g_4 C_2}{g_1 C_1 C_2} \right) \tag{8}$$

DDCCTA based shapers

DDCCTA [25]-[27], is relatively new active building block, employs DDCC [26] as input block which is followed by a TA. It has all the good properties of CCII and OTA, and special properties of DDCC such as easy implementation of differential and floating input circuits [26]. The DDCCTA symbol is shown in Fig. 6 and its terminal characteristics in matrix form are given by (9).

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ V_X \\ I_Z \\ I_{O1-} \\ I_{O2-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -g_m & 0 & 0 \\ 0 & 0 & 0 & 0 & -g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ V_Z \\ V_{O1-} \\ V_{O2-} \end{bmatrix} \tag{9}$$

where $g_m$is transconductance of the DDCCTA. The CMOS implementation of DDCCTA [26] is given in Fig. 7. It comprises of a DDCC block (Md1–Md12) [26] which is followed by transconductance amplifier (Md13–Md22). The value of transconductance (g_m)is expressed by (10) which can be can be adjusted by varying bias current I_{Bias}.

$$g_m = \sqrt{2\mu C_{ox}(W/L)_{15,16} I_{Bias}} \tag{10}$$

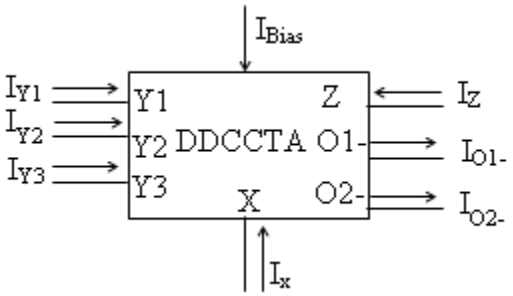

Fig 6. Symbol of proposed DDCCTA

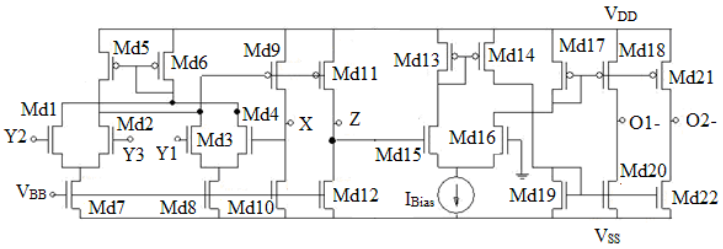

Fig 7. CMOS implementation of DDCCTA

The DDCCTA based voltage and current mode shaper circuits are proposed respectively in sections 3.1 and 3.2.

DDCCTA based voltage mode shaper

In this section n^{th} order voltage mode shaper based on DDCCTA is proposed. The circuit is shown in Fig. 8 which employs *(n+1)* DDCCTAs, *(n+1)* grounded capacitors, and three resistors. The differentiator employs one DDCCTA, one grounded capacitor and two resistors while *n* integrators employ *n* DDCCTAs, *n* grounded capacitors and one grounded resistor. The transfer function of theproposed n^{th} order shaper and itsoperating

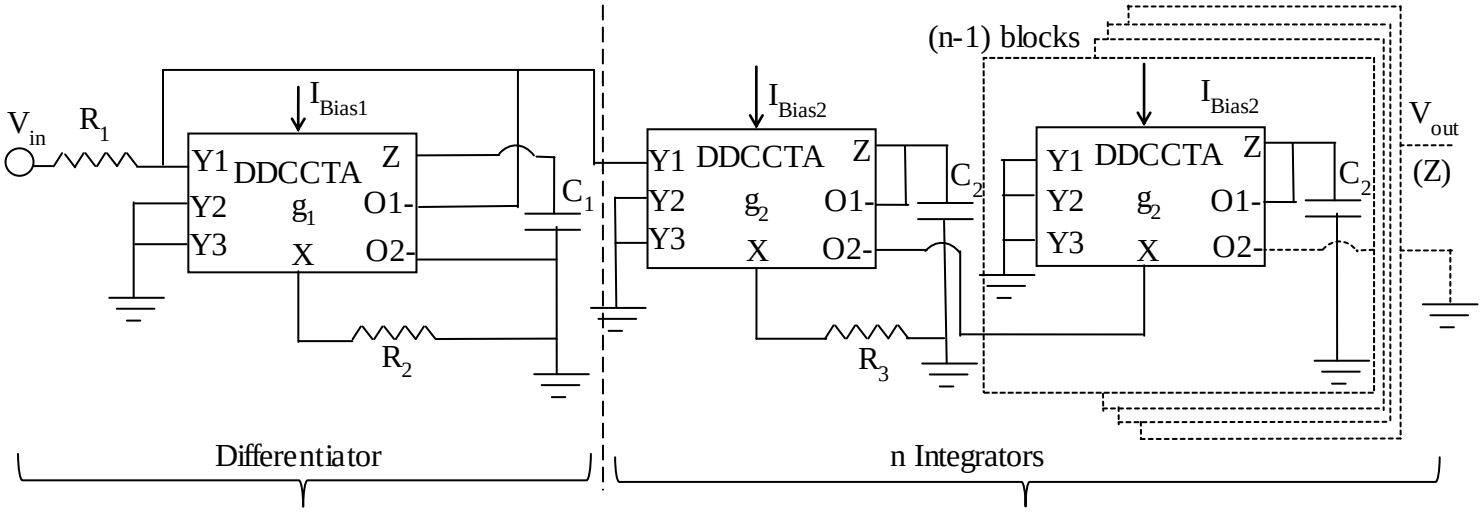

Fig. 8. Proposed DDCCTA based n[th] order voltage mode shaper

bandwidth is given by (11) and (12) respectively.

$$T(s)_{VM\_DDCCTA} = \left(\frac{s\frac{R_2C_1}{g_1R_1}}{1+s\frac{R_2C_1}{g_1R_1}}\right)\left(\frac{\frac{1}{\sqrt[n]{g_2R_3}}}{1+s\frac{C_2}{g_2}}\right)^n \quad (11)$$

$$BW_{VM\_DDCCTA} = f_{\text{int}} - f_{diff} = \frac{1}{2\pi}\left(\frac{g_2R_2C_1 - g_1R_1C_2}{R_2C_1C_2}\right) \quad (12)$$

$$T(s)_{CM\_DDCCTA} = \left(\frac{s\frac{R_2C_1}{g_1}}{1+s\frac{R_2C_1}{g_1R_1}}\right)\left(\frac{\frac{-1}{\sqrt[n]{R_3}}}{1+s\frac{C_2}{g_2}}\right)^n \quad (13)$$

$$BW_{CM\_DDCCTA} = f_{\text{int}} - f_{diff} = \frac{1}{2\pi}\left(\frac{g_2R_2C_1 - g_1R_1C_2}{R_2C_1C_2}\right) \quad (14)$$

DDCCTA based current mode shaper

Fig. 9 shows the proposed n^{th} order DDCCTA based current mode shaper. It uses *(n+1)* DDCCTAs, *(n+1)* grounded capacitors and three grounded resistors. The differentiator employs one DDCCTA, one grounded capacitor and two grounded resistors while *n* integrators employ *n* DDCCTAs, *n* grounded capacitors and one grounded resistor. The transfer function of the n^{th} order DDCCTA based current mode proposed shaper and its operating bandwidth is given by (13) and (14) respectively.

Simulation Results

The theoretical proposition has been verified through SPICE simulations using TSMC 0.25µm CMOS process model parameters. The CMOS schematic of Fig. 3 and Fig. 7 is used for CDTA and DDCCTA respectively, a part of CDTA schematic (Mc18-Mc26) is taken for TA. The aspect ratio of all the transistors for CDTA and DDCCTA is given in Table 1. The power supply voltages of V_{DD} = -V_{SS} = 1.8 V are used uniformly for all circuits and V_{BB} = -0.8V is taken for DDCCTA based shapers. The CDTA and DDCCTA based first order shapers

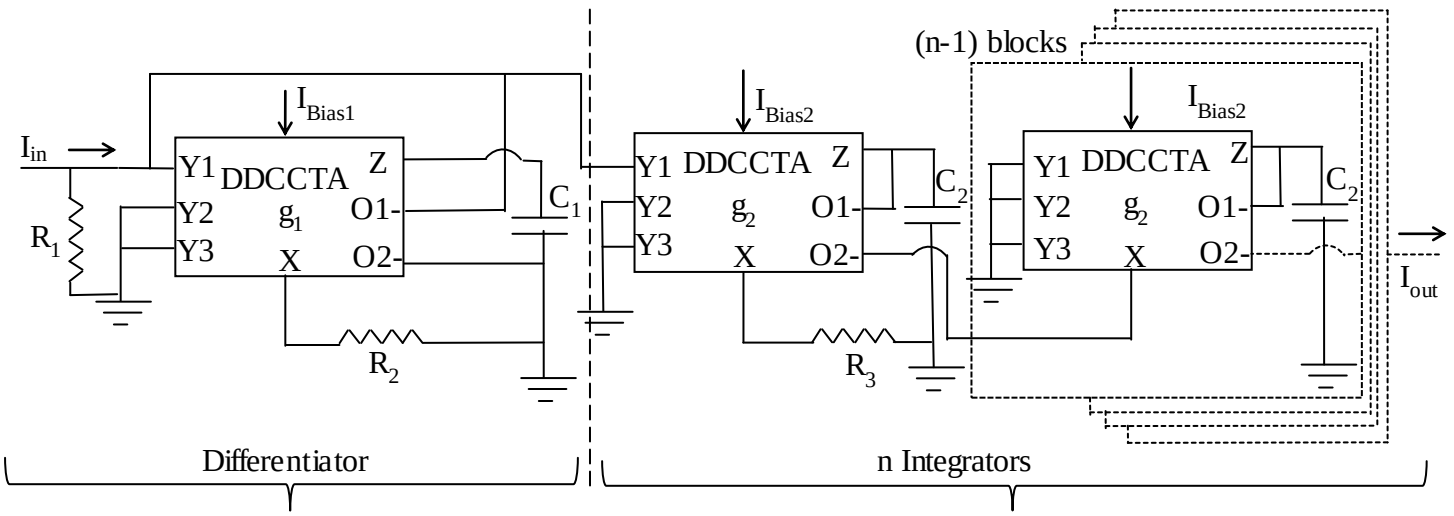

Fig 9. Proposed DDCCTA based n[th] order current mode shaper

Table 1. MOS Dimensions of CDTA and DDCCTA

CDTA		DDCCTA	
MOSFETs	*W(µm)/L (µm)*	*MOSFETs*	*W(µm)/L(µm)*
Mc26	7.0/0.7	Md5,Md6,Md13, Md14, Md17-Md22	5/0.5
Mc1	9.8/0.7	Md9,Md11	8.5/0.5
Mc2, Mc3, Mc13,Mc16, Mc17	10.5/0.7	Md1,Md2, Md3,Md4	10/0.5
Mc19, Mc21	16.1/0.7	Md7,Md8,	27.25/0.5
Mc6, Mc20	28.0/0.7	Md15,Md16	27/0.5
Mc8, Mc10, Mc18	28.7/0.7	Md10,Md12	44/0.5
Mc15, Mc12, Mc5	35.0/0.7	-	-
Mc4, Mc14	42.0/0.7	-	-
Mc22, Mc23, Mc25	56.0/0.7	-	-
Mc24	58.8/0.7	-	-
Mc7, Mc9, Mc11	70.0/0.7	-	-

are designed with operating bandwidth of 340KHz and 425KHz respectively. The circuit parameters for CDTA and DDCCTAbased voltage and current mode shapers are listed in Table 2. The frequency response of proposed CDTA and DDCCTA based first order shaper topologies in voltage and current mode is given in Fig. 10.

The transient behaviour of proposed shapers is also studied by applying input signals of frequencies 10KHz, 100KHz and 3MHz, each having an amplitude of 50mV each. Fig. 11 shows the input and output waveform along with their frequency spectrum for CDTA based first order voltage mode shaper. It may clearly be noted that the CDTA based voltage mode shaper allows only 10KHz and 100KHz to pass and significantly attenuates 3 MHz signal Similar responses for other shapers were also obtained.

Performance Evaluation

The performance of proposed topologies is compared in terms of total harmonic distortion, power dissipation, dynamic range, signal to noise ratio (SNR) and output noise. The total harmonic distortion (THD) and signal to noise ratio (SNR) of proposed shapers are shown in Figs. 12 and 13 respectively.

The total performance characteristics of proposed first order shapers are recapitulated in Table 3. Furthermore, performance of first order CDTA and DDCCTA based current mode shapers is compared with already existing second order CCII and OTA based LC ladder shaper topologies in terms of power dissipation, THD, Dynamic range and SNR and is given in Table 4.

Table 2. Circuit Parameters of CDTA and DDCCTA based first order shapers

Circuit Parameters	CDTA Voltage mode	CDTA Current mode	Circuit Parameters	DDCCTA Voltage mode	DDCCTA Current mode
I_{Bias1}, I_{Bias2}	1.20µA	2µA	I_{Bias1}	100µA	10µA
I_{Bias3}, I_{Bias4}	0.005µA	0.04µA	I_{Bias2}	10µA	10µA
C_1	50pF	40pF	R_1	1KΩ	5.5KΩ
C_2	80pF	100pF	R_2	100KΩ	40KΩ
R_1	20KΩ	-	R_3	7.2KΩ	5KΩ
R_2	20KΩ	-	C_1	100pF	100pF
-	-	-	C_2	50pF	65pF

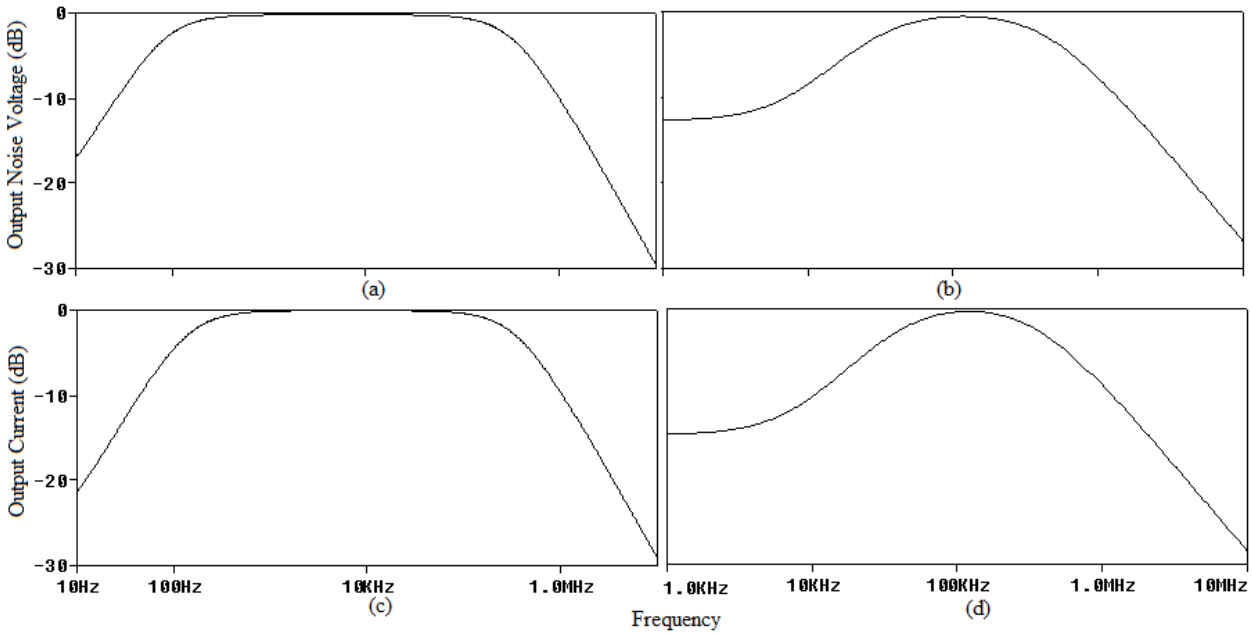

Fig. 10. Frequency Response of (a) CDTA and (b) DDCCTA based voltage mode; (c) CDTA and (d) DDCCTA based current mode first order shaper.

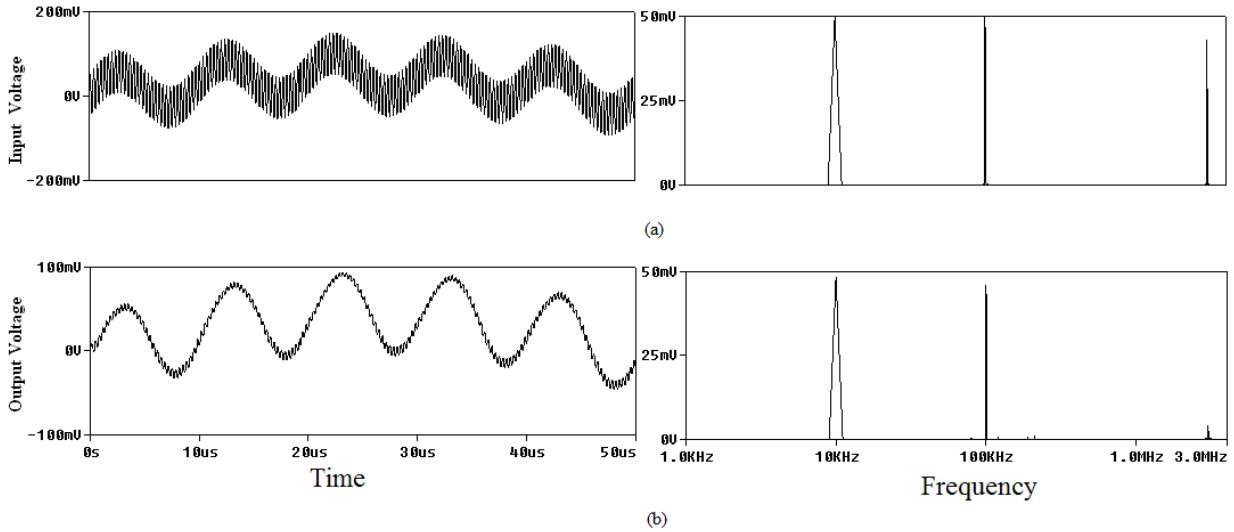

Fig. 11. (a) Input and its frequency spectrum (b) Output and its frequency spectrum

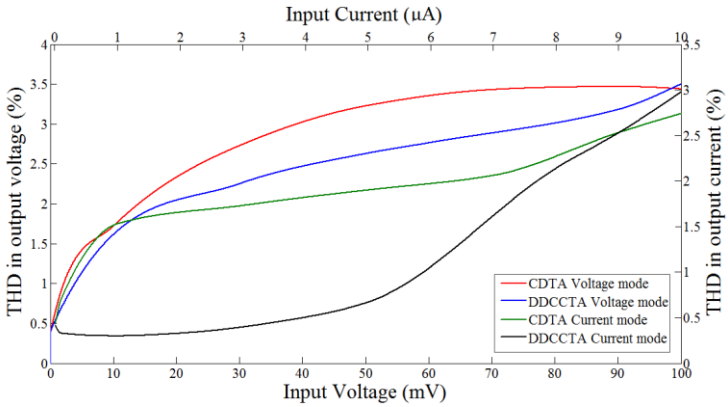

Fig. 12. THD of proposed shaper configurations

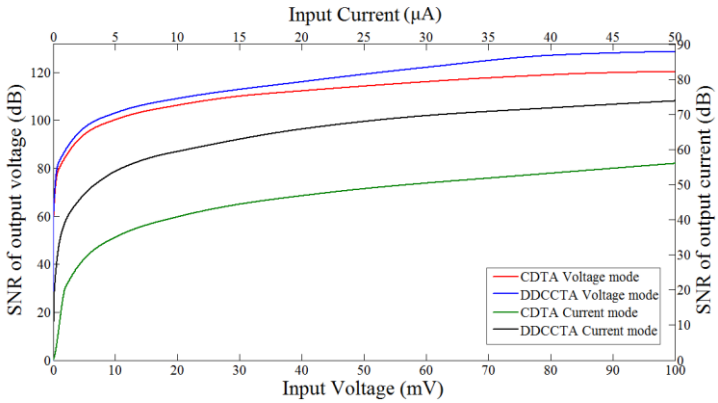

Fig 13. SNR of proposed shaper configurations

The DDCCTA based current mode shaper proved to be optimum concerning the dynamic range and SNR. The power dissipation of OTA based LC ladder shaper is least while it has maximum THD. The CCII LC ladder shaper has the minimum THD while it suffers from the drawback of high power dissipation. The CDTA based current mode shaper has low power dissipation, THD, dynamic range while high SNR value. The comparison proves that CDTA and DDCCTA based shapers have advantageous performance features over CCII and OTA based shapers.

Conclusion

In this paper, CDTA and DDCCTA based voltage and current mode S-G shaper circuits are presented. The shaper topologies use grounded capacitors and are suitable from integration point of view. The simulation results are included to demonstrate the workability of the circuits. The performance is characterized in terms of THD, power dissipation, dynamic range, SNR and output noise. The CDTA-based current and voltage mode shapers proved to be optimum concerning the power dissipation and total harmonic distortion (THD) while the DDCCTA-based current and voltage mode shapers appear to be the optimum concerning the dynamic range and signal to noise ratio (SNR). The output noise voltage of CDTA-based shaper is less than DDCCTA-based shaper when operated in voltage mode while DDCCTA-based shaper proved to have lesser output noise voltage when operated in current mode. The performance comparison of CDTA, DDCCTA, CCII and OTA based shapers proves that CDTA and DDCCTA based shapers have advantageous performance features over CCII and OTA based shapers.

Table 3. Performance Characteristics of CDTA and DDCCTA based first order shapers

Performance Parameters	CDTA Voltage mode	CDTA Current mode	DDCCTA Voltage mode	DDCCTA Current mode
THD (at 100mV/10µA)	3.44%	2.74%	3.50%	2.98%
Power Dissipation	0.37mW	0.62mW	1.88mW	1.42mW
DynamicRange (THD = 1%)	17.16dB	16.06dB	59.41dB	54.99dB
SNR (at 100mV/50µA)	120.20dB	56.00dB	128.60dB	73.80dB
Max. Output Noise Voltage	262.20nV	194.20nV	360.00nV	38.00nV

Table 4. Comparison of CCII, OTA, CDTA and DDCCTA based current mode shapers

Performance Parameters	CCII LC Ladder [20]	OTA LC Ladder [20]	CDTA Current mode	DDCCTA Current mode
Power Dissipation	5.50mW	0.13mW	0.62mW	1.42mW
THD (at 10μA)	0.32%	5.62%	2.74%	2.98%
DynamicRange (THD = 1%)	35.00dB	32.00dB	16.06dB	54.99dB
SNR (at 50μA)	40.00dB	38.00dB	56.00dB	73.80dB

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