Reversible Sequential Circuits – A Review

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ABSTRACT

VLSI Industry is moving at high speed towards miniaturization. With miniaturization it faces a problem of power and heat dissipation. Thus we need a superior technology that circumvents this problem. Solution is implementing Reversible logic. A lot of research has been already done in the field of reversible computing. This paper presents a review of such reversible sequential circuits in literature from basic elements to complex circuits.

Introduction

Reversible logic has shown potential to have extensive applications in emerging technologies such as quantum computing, optical computing, quantum dot cellular automata as well as ultra low power VLSI circuits. Recently, several researchers have focused their efforts on the design and synthesis of efficient reversible logic circuits. Reversible logic has been considered as an important issue for designing low power digital circuits. This has led many researchers to take reversible logic very seriously in building important circuits related to advance computing, low power CMOS design. The main idea of reversible logic is to allow the construction of reversible computers by using components which preserve information content, and can thus potentially be run backwards. Hence, by implementing reversible designs of computer hardware significant amount of heat can be reduced.

According to Landauer's principle, the loss of one bit of information dissipates $kT\ln 2$ joules of energy where k is the Boltzmann's constant and T is the absolute temperature at which the operation is performed [1]. Later Bennett, in 1973, showed that in order to avoid $kT\ln 2$ joules of energy dissipation in a circuit it must be built from reversible circuits [2]. According to Gordon Moore [3], shrinking the dimensions on integrated structures makes it possible to operate the structure at a higher speed for the same power per unit area. As more and more components are getting packed onto the chip, power dissipation in the present day computer is becoming very high. This heat dissipation extremely reduces the performance and lifetime of the circuits. The solution is to use revolutionary technology which enables extremely low power consumption and heat waste in computing- a reversible logic.
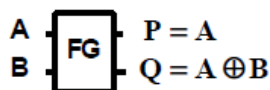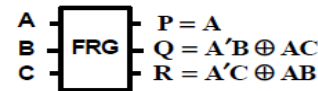

Feynman gate

Reversible circuits do not lose information and reversible computation in a system can be performed only when the system consists of reversible gates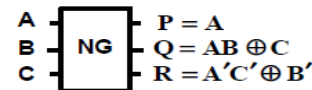. Some basic reversible gates are shown below which includes Feynman Gate(FG), Toffoli Gate(TG), Fredkin Gate(FRG), New Gate(NG).
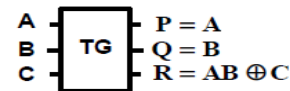

: Toffoli gate

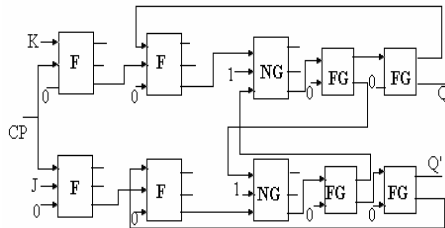: Fredkin gate

: New gate

Firstly, in reversible circuit there should be no fan-out, that is, each output will be utilized only once. Secondly, for each input template there should be a unique output template. eversible logic circuits are classified into reversible combinational and reversible sequential circuits. A reversible logic circuit should be designed using minimum number of reversible logic gates and with minimum number of constant inputs [4-7]. It has been shown that both the combinational as well as the sequential circuits can be designed using reversible logic gates. Reversible logic synthesis of sequential logic differs from combinational logic in that the output of the logic device is dependent not only on the present inputs to the device, but also on past inputs; i.e., the output of a sequential logic device depends on its present internal state and the present inputs.
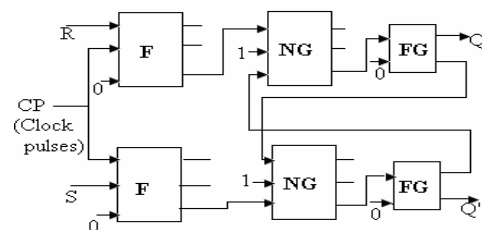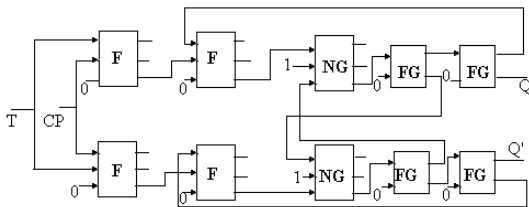

Reversible RS Flip Flop[8]

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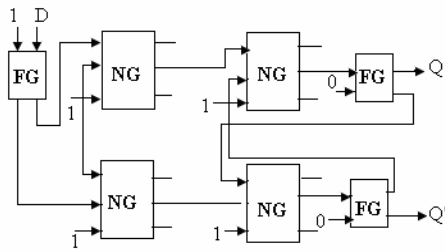
Reversible D Flip Flop[8]

Reversible JK Flip Flop[8]

Reversible T Flip Flop [8]

The important reversible gates used for reversible logic synthesis are Feynman Gate, New Gate and Fredkin gate[8]. Himanshu Thapliyal and M.B Srinivas in their paper provide the initial threshold to building of more complex system having reversible sequential circuits as a primitive component and which can execute more complicated operations using quantum computers.

Himanshu Thaplial gives Novel Reversible Flip Flops using Feynman Gate, New gate and Fredkin Gate. The designed FFs are highly optimized in terms of number of reversible gates and garbage outputs.

Himanshu Thapliyal and Nagarajan Ranganathan have presented novel designs of reversible latches which are optimized in terms of quantum cost, delay and garbage outputs [9]. They have shown that the choice of reversible gates and the design approach to carefully select a reversible gate for implementing a particular logic function will significantly impact the quantum cost, delay and garbage outputs of the reversible design.

Abu Sadat Md. Sayem, Masashi Ueda have proposed the reversible design of D-Latch nd JK Latch[10]. In this paper they have proposed optimized design of reversible sequential circuits in terms of number of gates, delay and hardware complexity. They have designed the latches with a new reversible gate and reduced the required number of gates, garbage outputs, and delay and hardware complexity. As the number of gates and garbage outputs increase the complexity of reversible circuits, this design will significantly enhance the performance.

Block diagram of Sayem Gate
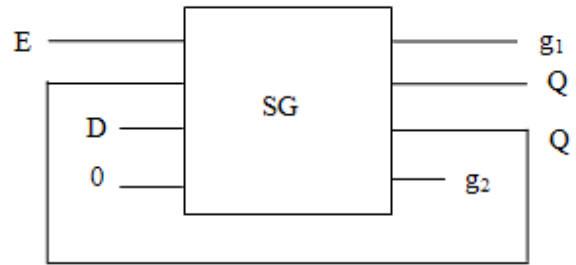
Design of D-Latch Using Sayem Gate
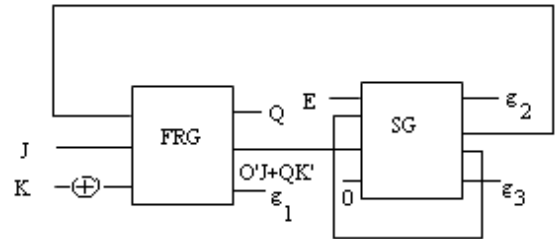
Design of reversible JK Latch

Latches are important memory element. Sayem has optimized these latches .Thus this optimization results in great contribution in designing logic circuits with memory and sequential elements. They have given the lower bounds for both the design in terms of number of gates and delay. They have proposed a new reversible gate which can contribute significantly in reversible logic community.

Md. Belayet Ali , Md. Mosharof Hossin and Md. Eneyat Ullah have proposed a new reversible gate and have designed RS flip flop and D flip flop by using their proposed gate and Peres gate. The proposed designs are better than the existing proposed ones in terms of number of reversible gates and garbage outputs. The resulting reversible sequential circuits are more cost competent[11].

K.Prabhakaran and V. Vidyadevi in their paper gives the reversible realization of 4-bit synchronous counters by using proposed reversible gates and the existing one. As far as it is known, this is the first attempt to apply reversible logic to synchronous counter design. They have proposed a new conservative reversible gate[12]. This gate can be used to produce multiple copies of a signal. The proposed synchronous counter designs have the applications in building reversible ALU, reversible processor etc. This work forms an important move in building large and complex reversible sequential circuits for quantum computers.

Sujata S. Chiwande , Shilpa S. Katre, Sushmita S. Dalvi; Jyoti C Kolte ,in their paper, have proposed comparison of synchronous & asynchronous counter using Sayem reversible gate[13]. In the comparative analysis they have compared the number of gates, garbage output & power dissipation.

Conclusion: From this review, it has been observed that reversible logic gates can be successfully used to implement sequential circuits. Further these circuits can be optimized for the number of reversible gates, garbage outputs, quantum cost, flexibility etc. The future work can be done to develop efficient reversible counters and reversible controller circuits. Further transistorised implementation of these circuits is another field which can be explored.

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