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Source degraded LNA Design in 0.13µm CMOS process for Personal Wireless Area Network

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ABSTRACT

This paper presents the results of a RF receiver front-end design used in Personal Wireless Area Network (PWAN) and implemented in a 0.13µm CMOS process with source degenerated amplifier. Device models were used in MULTISIM and MATLAB Particle Swamp Optimization implementation to iteratively find a solution to optimal component values for user LNAtopology. To demonstrate the design methodology, a sub-mW fully integrated narrow-band sourcedegenerated cascode RF LNA is designed and simulated in a standard 0.13µm CMOSprocess to operate in the 2.4GHz band. The LNA achieves a voltage gain of 24 dB,noise figure (NF) of 1.4 dB, from a 4.4 mA supply current.

Introduction

Personal area network wireless technology will allow seamless interconnectivity among devices. Computers and personal digital assistants (PDAs) will share files and synchronize databases remotely; laptop PCs will access e-mail by linking to nearby cellular phones; and wireless headsets will permeate the cellular phone market to simplify hands-free operation. Applications for this technology are already underway in many R&D labs around the world. The technology's potential is limitless when one considers the growing sector of information appliances that would benefit from wireless connectivity. LNA monolithic microwave integrated circuits (MMICs) for automotive wireless systems have been implemented by using compound semiconductor processes such as GaAs(. R. Eye,et al,2003), InP (S. Weinreb et al,1999) or SiGe(L. Wang,et al,2006) due to their higher cutoff frequency and lower thermal noise than CMOS process. However, recent advance in CMOS process has scaled down the channel length of FET's to several tens of nanometer. Due to shortening the channel length of CMOS transistors, the maximum oscillation frequency is increased up to several hundred Giga-hertz (C. H. Doan et al, 2005). Therefore, the performance of CMOS transistors is becoming comparable to that of compound semiconductor processes. This motivates implementing low cost millimeter-wave circuits like gigabit wireless personal area network (WPAN)(T.W. Huang et al,2008) by using advanced CMOS processes.

Personal Wireless Area Network Protocol Specifications

PWAN technology was originally proposed by Ericsson as a ''cable replacement technology'' has the following performance standard.

Parameter	Specification	Units
Frequency Range	2402-2480	MHz
Channel Spacing	1	MHz
Number of channels	79	
Multiple Access Method (Pseudo random frequency hop)	1600	Hops/s
Duplex Method	Time-division demultiplexing	
Modulation method	Gaussian frequency shift keying	
Receiver Sensitivity(min.signal level)	-70	dBm
Maximum usable level	-20	dBm

Performance metrics

Maximum power transfer theorem.

Maximum power transfer theorem states that the transmitted power to load is maximized when the source impedance is the complex conjugate of the load impedance.

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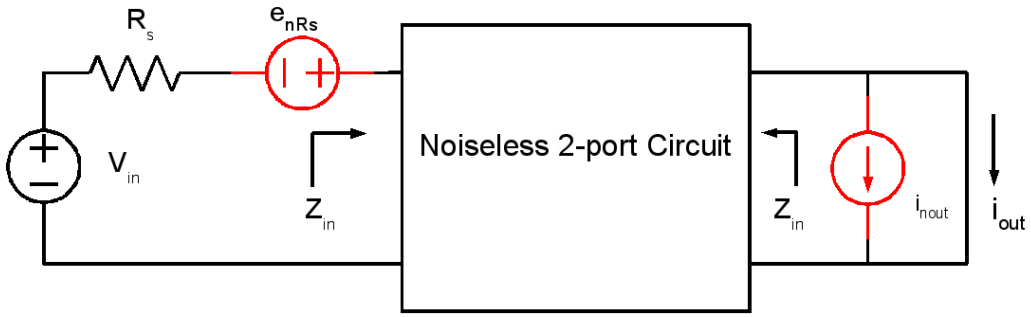
$$Z_S = G_S + jB_S \Rightarrow Z_{inp} = \overline{Z_S} = G_S - jB_S \quad \text{..... (1).}$$

The source impedance is selected to be 50Ω, a value that is associated with coaxial cables.

a) Noise Figure (NF) and Noise Factor (F).

$$F = \frac{SNR_i}{SNR_o}$$



..... (2).

$$NF = 10\log(F) \quad \text{.....(3)}$$

Fig.1.A model of a Noiseless 2-port device with input and output circuits

$$SNR_i = \frac{|\alpha|^2 v_i^2}{e_{nRs}^2} \quad \text{.....(4).}$$

$$SNR_o = \frac{|\alpha|^2 |G_m|^2 v_i^2}{|\alpha|^2 |G_m|^2 \overline{e_{nRs}^2} + \overline{i_{nout}^2}} \quad \text{.....(5).}$$

$$F = 1 + \frac{\overline{i_{nout}^2}}{|\alpha|^2 |G_m|^2 e_{nRs}^2} \quad \text{.....(6).}$$

For MOSFETs, noise is associated mainly with the drain and gate and the two types of noise are correlated. The drain noise is due to thermal and captures release processes in the channel. The thermal channel noise current is expressed as:

$$\overrightarrow{i_{nd}^2} = 4kT\gamma g_{do}\Delta F \quad \text{.....(7).}$$

Where γ is the excess noise factor.

The flicker noise, 1/f, whichis also associated with drain does not present problems when the device operates in high frequencies and therefore not a problem for the LNA.

The noise associated with the drain is the thermal noise due to intrinsic gate resistance as well as routing. The other is the induced gate noise due to quantum nature of charge. This causes random variation of potential along the channel. The induced gate noise expression is given as:

$$\overline{i_{ng}^2} = 4kT\delta g_{do}\left(\frac{f\alpha}{\sqrt{5}f}\right)\Delta f \quad \text{.....(8)}$$

where,δ is the noise coefficient.

CMOS Narrow Band Amplifier design.

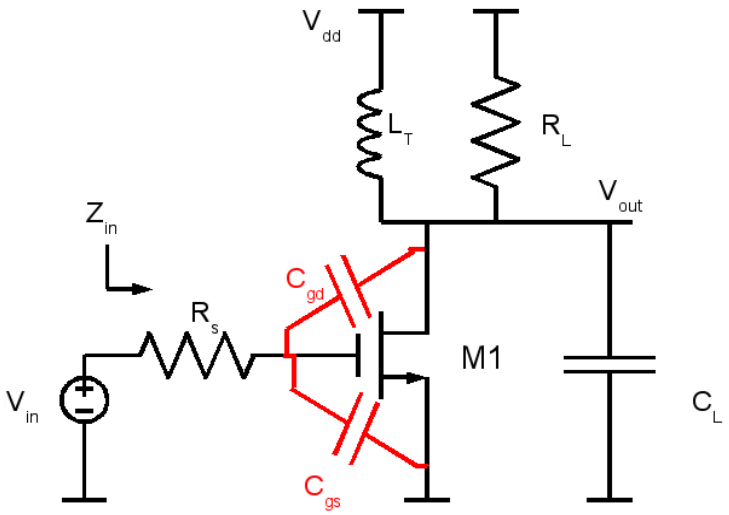


Fig.2.Sigle-stage MOSFET design showing g-d and g-s capacitances.

Input impedance for the stage can be expressed as:

$$Z_{in}(\omega) \approx \frac{1}{j\omega C_{gs}} \left\| j\omega C_{gs} \right\| \frac{-1}{\omega g_m C_{gd} L} \quad \text{.....(9).}$$

Cascode topology

When a cascode device is added (as indicated in figure 3) the amplifier`s input and output are isolated and the input impedance becomes purely capacitive.

$$Z_{in} = \frac{1}{j\omega C_{gs}} \left\| \frac{1}{j\omega C_{gd}(1 + g_{m1}/g_{m2}} \right. \quad \text{.....(10)}$$

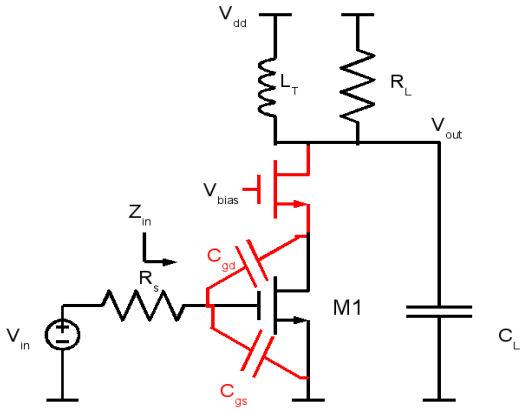


Fig.3.Cascaded MOSFETs

The isolation between input and output will not be perfect.Cascode will still reflect the load impedance to its input at resonance due high output conductance of 0.13µm CMOS devices.

$$R_{in} = \frac{R_L + r_0}{r_O(g_m + g_{mb})} \quad \text{.....(11).}$$

Source degenerated CMOS LNA.

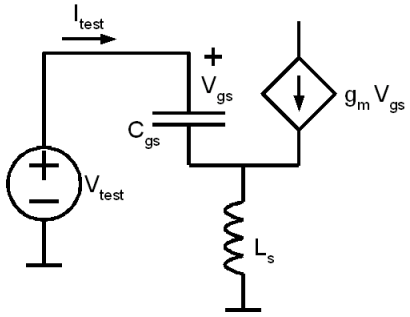


Fig.4.Equivalent circuit for source degenerated amplifier.

The input impedance for the LAN can be expressed as:

$$\frac{v_{test}}{i_{test}} = Z_{in}(s) = \frac{1}{sC_{gs}} + sL_S + \frac{g_m}{C_{gs}}L_s \quad \text{.....(12).}$$

This is the impedance expression for a series resonant circuit. This circuit should resonate at $\omega_o$so that the impedance is purely resistive mid-band. The extra inductor,L_g, is introducedas shown in figure 5.This will bring the resonance frequency to mid-band.

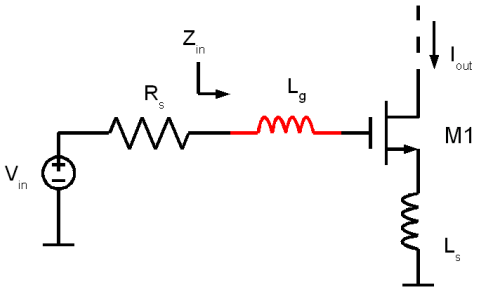


Fig.5.Impedance matching for LNA extra gate resistor, $L_g$for resonance matching.

$$Z_{in} = \frac{1}{sC_{gs}} + s(L_s + L_g) + \frac{g_m}{C_{gs}}L_s \quad \text{.....(13)}$$

.

$$\omega_o = \frac{1}{\sqrt{(L_s + L_g)C_{gs}}} \quad \text{.....(14)}$$

Analysis

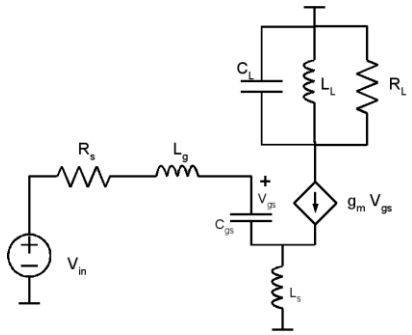


Fig.6.Equivalent circuit for the determination of circuit parameters

The following values were adopted for simulation of the circuit using figure 6 above;

a) Centre frequency of LNA:f_o=2.45GHz.

b) Transistion frequency of 0.13µm NMOS:f_t=72GHz;

c) Correlation factor of –j0.55;

d) Excess noise factor for the drain current: γ=3;

e) Induced gate noise coefficient:δ=6;

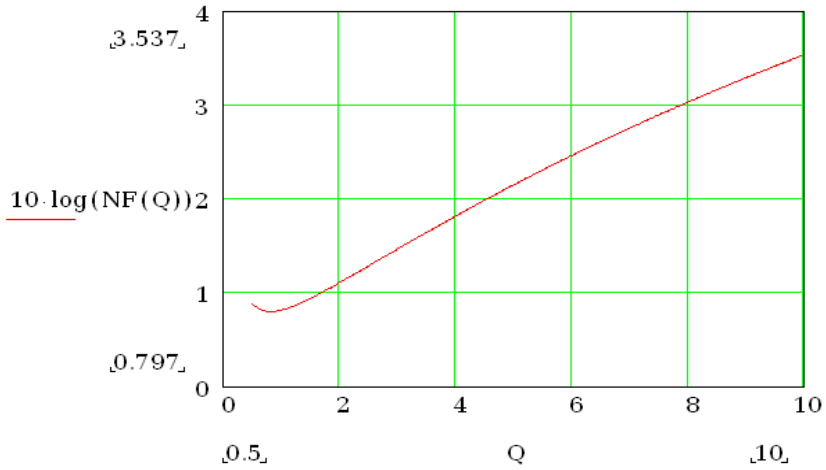


Fig.7.A simulated graph from which the quality factor (Q) was established.

Results and Conclusion

The final design had the values depicted in the table below.

Parameter	Value	Unit
Noise Figure	1.4	dB
Voltage Gain	24	dB
Input Impedance.	36	Ω
Gate Width	196	µm
L_s	1.5	µH
L_L	1.7	nH
L_g	14.8	nH
Supply Current	4.4	mA

The low noise amplifier (LNA) is a crucial part in RF receiver. It is designed for selecting andamplifying weak signals in certain frequency, reducing noise, and providing an appropriate working condition for the following mixer. We first analyze some parameters, such as noise figure, input impedance match, gain, and linearity that reflect the quality of LNA. Then we designed an inductive source degenerated cascode LNA with the working frequency of 2.4GHz. The simulation results got from MATLAB and MULTISIM indicate that the values of the components are appropriate and the performance of the designed LNA is acceptable.

	Typical Values [12]	LNA performance in recent reported designs (2.4GHz or beyond)					
		LNA in Fig. 1	LNA in Fig. 5	[13]	[5]	[11]	[11]
NF	2 dB	2.2 dB	2.4 dB	2.5 dB	2.4 dB	2.5 dB	3 dB
IIP_3	-10 dBm	1.3 dBm	-3.4 dBm	2 dBm		-10 dB	-10 dB
1-dB Compression	-20 ~ -25 dBm	-18 dBm	-21 dBm	-12 dBm			
Power Gain	15 dB	15 dB	20 dB	19.9 dB	19 dB	22 dB	18 dB
Input Return Loss	-15 dB	-17 dB	-19 dB		-10 dB		
Output Return Loss	-15 dB	-23 dB	-21 dB				
Reverse Isolation	20 dB	24 dB	35 dB	47.8 dB			
Stability Factor	> 1	1.4	3.6				
Frequency		2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz	2.5 GHz	3 GHz
Power Dissipation		4.8 mW	7.2 mW	14.7 mW		12 mW	12 mW
Process		0.25 µm	0.25 µm	0.35 µm	0.5 µm	0.35 µm	0.35 µm
Supply Voltage		3.3 V	3.3 V	2 V	3 V	1.5 V	1.5 V
Year		2001	2001	2001	1999	1999	1999

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