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Novel Subthreshold and Gate Leakage Reduction Techniques for 6t- Sram Cell

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ABSTRACT

Power has been an important issue for the present day microelectronic circuits of Soc designs. In the entire phase of design controlling power and dealing with power dissipation is very important. There are six leakage components in a MOS transistor. About 50 % of the total power consumption is through leakage components alone. Out of this 40 % power dissipation is through transistors. Out of them subthreshold leakage and gate leakage are of important concern for sub 100 nm devices. In this work we presented the main leakages in a 6T- SRAM cell. Later we presented an existing variable body biasing method and its performance. We proposed two novel methodologies HSVR, GSVE to reduce the subthreshold and gate leakage components. These methods are toplogy based leakage reduction methods applied for leakage reduction in the circuit level. We observed considerable reduction of both the components through the proposed methods.

Introduction

Static RAM is a volatile type of semiconductor memory used to store data as long as power is on. SRAM (Fig 1) is widely used in latest designs to increase the speed of operations in Microprocessor and other computing areas. In the case of DRAM as the charge leaks and data is lost over a period of time, a refresh operation is required for every few milli seconds. But for SRAM, no such operation is required which is primary advantage of it. Embedded RAM's with supply voltage of 0.6 V is reported in [1] through research and development of 16 MB DRAM have become prominent in present SoC technologies. In development of RAM's we need to face challenges from four directions [2-4] to minimize the leakage current in the RAM cell.

a) Maintaining appropriate Signal voltage and Signal charge in the RAM cell.

b) Minimize the RAM cell area.

c) Minimizing the fluctuations of speed caused by change of threshold voltage of the MOS device in RAM cell due to CMOS scaling effect.

Among the above challenges reduction of leakage current is important issue in the design of RAM cell.

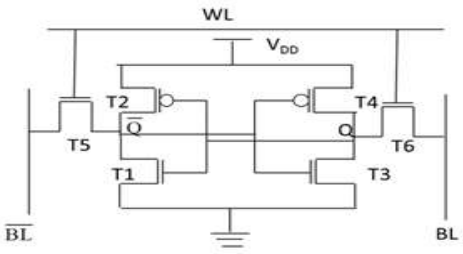

Fig 1 Schematic of 6T-SRAM cell

When the SRAM cell is selected the value is latched into the cross coupled inverters. The SRAM cells are arranged in a Matrix and each cell can be addressed individually. There are three operations possible for SRAM cell, Read, Write and Hold. In holding the value the access transistors are off and bit and word line are asserted low. Using the bit line and its inverse increases the noise margin and good data integrity. The small voltage swings are detected by passing the values of bit line and its complement to a comparator [12].

Leakage mechanism in sram cell

In the earlier chapters we identified that there are six types of leakage components in a MOS transistor. In a typical 6T-SRAM cell two major leakage components have shown their impact on the performance and power savings. They are Sub-Threshold leakage current and Gate Tunneling current. When the threshold voltage and oxide thickness is reduced the leakage current increases in the SRAM cell. Both the subthreshold and gate leakage current effect the RAM cell performance both during the standby and runtime. They not only affect the memory cell but also the control and peripheral circuitry of the memory. Hence it is important to reduce both the leakage components during the design phase. Reducing the sub-threshold leakage lies in the hands of the circuit design group while reducing the gate leakage current lies in the hands of process and fabrication group.

Sub-threshold leakage current in 6T-SRAM cell

Sub-threshold leakage current is observed in SRAM cell in two locations [5] as shown in Figure 2.a)Leakage current that flows between Transistors T2 and T1 (also between T4 and T3) between the power supply rails.b)Leakage current between the bit lines (via T5 and T6) and the Ground as shown in the figure. Though there are two bit lines in the SRAM cell the leakage through them varies according to the logic value stored in the SRAM cell. When SRAM cell writes logic 1, i.e. the gate voltage and drain voltage of T6 is same (VDD) hence potentially zero current flows through it.Similarly T3 is turned off for logic 1 stored in the SRAM cell hence both the transistors are in stack thus reducing the leakage current. Hence bit line leakage is reduced. But large leakage current flows through T5 and T1.Similarly when writing logic 0 the bit line leakage is reduced through the other path i.e T5 and T1. Subthreshold leakage occurs in the transistor in the weak

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inversion region i.e when $V_{GS} < V_{th}$. V_{th} reduction takes place due to many factors. When the supply voltage is to be reduced along with the technologies, the threshold voltage should be scaled proportionately. Similarly due to secondary effects of the short channel MOS transistor also the threshold voltage reduces.

The subthreshold leakage current increases exponentially with reduction in the V_{th}.In literature to reduce the sub-threshold leakage the V_{th} of all or certain transistors is increased. The limitation to this solution is the delay of read and write operations increase. For example if the V_{th} of T6 is increased either during fabrication process(additional doping in the channel area) or by body Biasing (by changing the reverse bias voltage of the body) the wake up time or response time of the transistor increased which effects the red and write cycles. The proposed method also increases the process complexity through additional masking steps. The write delay increases when the V_{th} of PMOS devices is increased while effect on read delay is negligible. The read delay increases when V_{th} of NMOS devices is increased while effect on write delay is negligible. Whereas increase of V_{th} of T5 and T6 affects both read and write delay. Reducing the threshold voltage is more beneficial when write delay is less than read delay caused by additional circuitry.

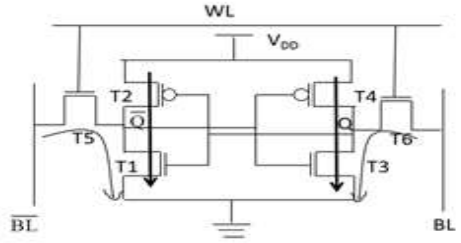

Fig 2. Leakage components in SRAM cell.

Gate Leakage in 6T- SRAM cell

The second leakage current observed in RAM cells is gate leakage current due to tunneling effect. Due to smaller technology dimensions of sub 100nm the thickness of the oxide should be scaled down to maintain good aspect ratio. This increases the electric field across the oxide so that the charge carriers (electrons and holes tunnel towards the gate terminal). In an NMOS transistor the electrons tunnel from the body/substrate towards positively biased gate terminal. This leakage component is observed both when the device is OFF and ON conditions. Hence reducing the effect of this component saves significant amount of power. For SRAM's used in modern computing SoC devices the number of read and write operations are more per unit time hence reducing gate leakage is very important area of research.

This tunneling current comprises of three components:

a) Tunneling current due to gate overlap region in source and drain regions.

b) Gate to Channel component.

c) Gate to Bulk Component

The part of Gate to channel current moves to source and drain. Among the above three components Gate to Bulk component is less than the other two for bulk CMOS technologies [6]. The overlapping tunneling component from source and drain is more predominant when the transistor is OFF while the Gate to channel tunneling component is predominant in ON condition. The overlap region is very small in area compared to the channel area hence gate leakage current is less in OFF state than in ON state[7]. To reduce the gate leakage one solution proposed is to use High-K dielectric materials or increase the thickness of the oxide. When SiO_2 is used as insulating material gate leakage is slightly is PMOS transistors [8]. Hence the leakage savings obtained through increasing the thickness is very small for PMOS transistors.In summary the subthreshold leakage component is dominant in T6, T4, T1 transistors while gate leakage is dominant in T3, T5, and T2. It doesn't mean the component doesn't exist in other transistors but negligible.

Existing Method-Variable Body Biasing Method

The architecture of the body biasing techniques is shown below in Fig 3 below. In this method two additional sleep transistors are added in both pull-up and pull-down network.to introduce body biasing effect the source of one PMOS device is connected to the body of the other PMOS device. Similarly the source of one NMOS device is connected to body of another NMOS device. The leakage reduction occurs both by sleep transistor effect and by body biasing effect. The PMOS transistors cannot conduct good V_{SS} value while NMOS transistors are not good at passing perfect V_{DD} value. To restore the logic in the sleep state PMOS is used in parallel in PDN while NMOS is used in parallel in PMOS network.

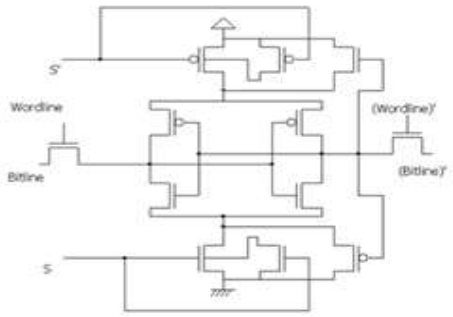

Fig 3. Schematic of Variable Body Biasing

The width of the PMOS transistors is made wider than NMOS transistors for equal rise and fall times. Due to minimum aspect ratio used in sleep transistors the leakage current reduces. In the active condition Sleep=1 and Sleep bar=0. Both the sleep transistors are ON and normal read and write operations can be performed on the SRAM cell. During the sleep mode sleep=0 and sleep bar =1 and both the sleep transistors are turned off. But due to the source of transistors tied to the body of the similar transistor the threshold voltage of the sleep transistor increases [11].As we know the increase in threshold voltage reduces the sub threshold leakage current of the transistor. Due to this the standby leakage current reduces through this approach. The purpose of additional transistors in the architecture is to retain the state in the sleep mode. To store logic one during sleep mode all the sleep transistors are off but the NMOS transistor connected parallel is the only source of power supply to the PDN. Similarly to restore logic zero the NMOS connected in parallel is the only source to Ground for PDN. The sub-threshold current is proportional to the width of the transistor, Gate voltage and threshold voltage and sub threshold swing. The circuit engineers propose leakage reduction methods by properly controlling the above parameters. In this approach the threshold voltage can be changed accordingly by changing the node voltages of the transistor. This approach is widely used in reduction of sub-threshold leakage currents in the literature. The area of the SRAM cell increases tremendously as four additional

transistors are added in this approach which is a severe limitation. For an array of SRAM cells this poses a big area penalty problem. We compared the performance of variable body bias method with our proposed methods.

High Supply Voltage Reduction Method (Hsvr)

To reduce the impact of sub-threshold and gate leakage currents we added a small additional circuitry between the original power supply and the latch of the SRAM cell (Fig 4). When the SRAM cell is in active mode (during Read and Write operations) a full swing V_{DD} is applied to the cell.

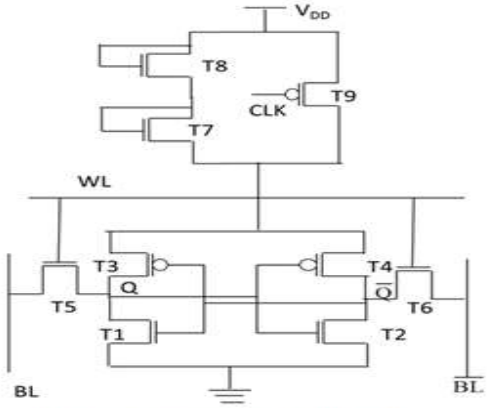

Fig 3. Schematic of HSVR method

The additional transistors provide a reduced voltage drop during the standby mode across T7, T8 and T9 network.T9 is operated through clock. During the ON condition we provide alternative path between V_{DD} and SRAM cell. In the standby mode the clock is off and T9 conducting. There is potential drop in T9 thus reducing the supply voltage to the SRAM cell. Where as in OFF condition the clock is held high thus creating high resistance between VDD and SRAM cell. The leakage current within each transistor is dependent on the value stored in the SRAM cell.Let us consider when logic 0 is stored in the cell, The gate leakage component in transistors T2,T5,T6 and T1 are considered because the component in T3 and T4 can be neglected because of PMOS nature. The gate leakage component is due to Edge Tunneling mechanism at source and drain edges (EDT). The Gate leakage is high in T1 is significant due to EDT.The subthreshold Leakage component is observed in OFF transistors of the SRAM cell i.e., T2 ,T3 and Access transistors T5 and T6.As the VDS value of the T6 is zero the subthreshold leakage component is less and can be neglected but it is maximum in the remaining Transistors (T2,T3,T5). Any Leakage reduction method should address the reduction in all these transistors.

Effect of HSVR on Sub-Threshold leakage reduction

In the inactive state a less voltage Vd<< VDD is applied to the source of T4 transistor hence the drain voltage of T4 and T2 reduces compared to the value when VDD is applied.

•As the Access transistor T5 is OFF in inactive state, the sub-threshold leakage current remains unchanged.

•Initially there is no sub-threshold leakage component in T6. But as logic value 0 is stored in the cell, an additional subthreshold leakage component is observed across it due to voltage drop at the source of it.

Effect of HSVR on gate leakage reduction

As T4 is conducting and the source voltage is reduced both the gate tunneling EDT components are reduced. When T4 is ON and the voltage at drain of T4 and T2 reduced, the gate voltage of T1 reduced. This reduces the EDT component of T1.As the V_{DS} value of T2 Reduces the gate leakage current reduces. The decrease in source voltage of T6 decreases one EDT component while leaving the other unchanged. (It is to be recalled that there are two EDT components of T6).Gate tunneling leakage across T5 remains unchanged as there is no voltage change on the bit bar line. As T3 is a PMOS transistor the leakage reduction is negligible. An additional gate leakage component is observed across T9 in the SRAM circuit.

Ground Supply Voltage Elevation Method (Gsve)

In contrast to the previous proposed method in which we reduced the higher supply voltage in this approach we raise the ground potential to reduce the sub-threshold leakage in the SRAM cell. As the ground potential is raised the voltage swing is reduced which in turn reduces the leakage current. As we know each transistor has different leakage components in standby mode the same analysis should be carried out as in the previous section. Three additional transistors are added between the ground potential and NMOS transistors of the SRAM cell. Transistor T9 acts like a control switch driven by the clock signal. Clock is enabled during the read and write operations so that full voltage swing is achieved. But during standby mode an alternative path is established between the ground and SRAM cell to raise the potential. This method is similar to diode footed cache design in which a high V_{th} transistor is used to raise the ground potential.

Effect of GSVE on Gate leakage reduction

As we increased the Ground Potential form 0V to Vs volts, For Transistor T1 there is increase in V_{GS} and V_{GD} values. This reduces the gate tunneling leakage current. For Transistor T2 the V_{GD} potential is increased thus sharply reducing the gate leakage component. There is no change in the gate leakage component for access transistors T5 and T6.but due to raise in drain potential of T1 an additional gate tunneling leakage component is observed across T5 which is penalty for the proposed method. An additional gate leakage component is observed in T9 which cannot be neglected due to the size compared to the NMOS transistors of the cell.

Effect of GSVE on Sub-Threshold leakage reduction

Due to the effect of additional sub-threshold leakage component in the SRAM cell the output performance degrades when the temperature in the circuit increase. It is to be remembered that there is exponential dependency of sub-threshold leakage component with temperature. The only way left to the circuit engineers to reduce this leakage component is by changing the gate, source and drain voltages.Due to increase in source voltage of T2, the sub-threshold leakage component has reduced as it is dependent on VGS value of the MOS transistor.The subthreshold leakage components in T3 and T5 are also reduced because of variation of node voltages in the circuits due to rise in the ground potential of the circuit.

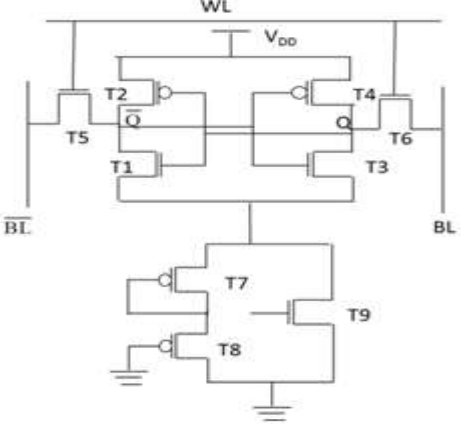

Fig 4. Schematic of GSVE method

Simulation And Results

In the present work we compared the performance of our proposed methods against the existing Variable body Biasing. For understand the leakage reduction through our proposed methods 70nm BPTM model files are simulated in Cadence Spectre. To measure the runtime leakage current we simulated the SRAM cell for 10 Read and Write cycles. During the standby mode the clock is not applied to the control switch of the cell thus reducing the VDD value in HSVR method and increasing the ground potential in GSVE method. The schematic of the conventional SRAM cell and HSVR and GSVE methods are shown in figures 5, 6, and 7

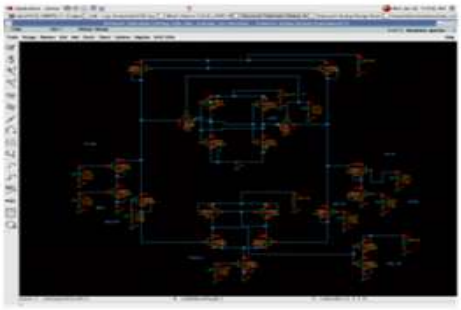

Fig 5. Schematic of conventional SRAM cell.

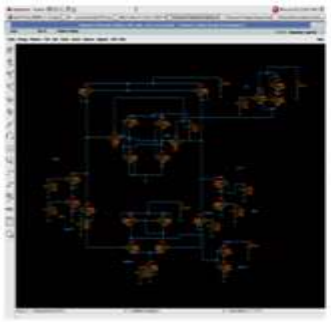

Fig 6. Schematic of HSVR method

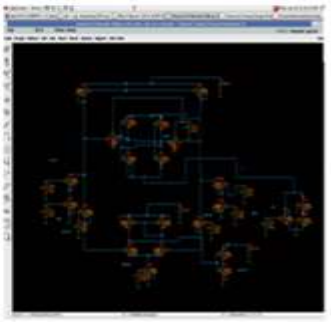

Fig 7. Schematic of GSVE method

The subthreshold leakage components and gate tunneling leakage components in each of the transistors with comparison between our proposed methods and conventional SRAM is given in Table 1.

Table 1. Leakage current in individual transistors of proposed methods and Variable body bias

Transistor	Leakage component (nA)	Conventional SRAM (nA)	HSVR-SRAM(nA)	GSVE-SRAM(nA)
T1	I_G	37.1	2.38	2.35
	I_{sub}	29.3	28.9	29.1
T2	I_G	13.9	1.14	1.08
	I_{sub}	16.8	2.38	1.79
T3	I_G	12.47	11.43	10.83
	I_{sub}	0.86	0.58	0.17
T4	I_G	23.31	2.49	3.46
	I_{sub}	0.56	0.56	0.29
T5	I_G	9.84	9.84	8.34
	I_{sub}	0.62	0.62	0.31
T6	I_G	19.5	18.43	19.21
	I_{sub}	0.64	0.92	0.61

The following conclusions can be drawn from the measured leakage current of different transistors comparing conventional SRAM and HSVR-SRAM. In T1 transistor the gate and subthreshold leakage components reduced to 6.5 % of the value in the conventional SRAM cell while subthreshold leakage component remains unchanged. In T2 transistor the gate leakage component is reduced to 8.2 % of the initial value while subthreshold leakage component reduced by 86 %.In T3 not much gate leakage current and subthreshold leakage current savings are observed. As it is a PMOS device the gate leakage can be neglected. In T4 transistor the gate leakage component reduced by 89% while subthreshold leakage reduction is not observed. In T5 transistor there is no reduction in gate leakage current as well as subthreshold leakage current.

Table 2. Leakage power comparison between Variable body Bias and HVSR, GSVE

	Standby Leakage (nW)	Runtime Leakage(nW)	Propagation Delay(ns)	Area (μm^2)
Conventional SRAM	83.6	74.5	3.031	14.31
Variable Body Biased SRAM	69.4	52.13	4.853	17.48
HSVR- SRAM	45.3	10.42	4.679	16.25
GSVE- SRAM	23.6	48.3	4.573	16.74

In T6 gate leakage component reduced by 4% while subthreshold leakage component increased by 40%. The following conclusions can be drawn from the measured leakage current of different transistors comparing conventional SRAM and GSVE-SRAM.In T1 the gate leakage component reduced to 7 % of its initial value in conventional SRAM cell but there is no change in the sub-threshold leakage component. In T2 gate leakage component reduced to 7.7 % of its value in conventional SRAM cell while subthreshold leakage component reduced by 89 % which is a significant value. In T3 subthreshold leakage current reduced by 80 % while gate leakage current reduced only by only 14%.In T4 the gate leakage current is reduced by 85 % while subthreshold leakage component reduced by 50 %.In T5 the gate leakage reduced by 15 % while subthreshold leakage current reduced by 50%.In T6 there is no reduction in gate leakage while subthreshold leakage reduced by 5% which is very less value. In addition to the above reduction in the leakage components an additional EDT gate leakage current is observed in T9 for HSVR method. Though we measured the leakage reduction for each individual transistor, the Resultant leakage value is calculated by the simulator and is given in Table 2. It is observed that HSVR method is best suited for reduction of gate leakage current while GSVE is suitable for reduction of sub-threshold leakage reduction. The standby leakage and active leakage, Area are compared with Variable Body Biasing methods versus the proposed methods are shown in table 2. From the above measured values the propagation delay of HSVR and GSVE is slightly higher than Conventional SRAM, less than variable body bias method which has four additional transistors added to the SRAM cell. Due to additional transistors there is slight increase in area for the proposed SRAM cells. In HSVR the runtime leakage current reduced by 86 % compared to conventional SRAM cell as gate leakage current reduced in most off the transistors when the cell is in the operating mode. In GSVE method the standby leakage current reduced by 72 %.

Conclusion

The present work analyzes the latest developments in low-power circuit techniques and methods with an emphasis on SRAMs. Many of reviewed techniques are applicable to other applications such as ASICs, DSPs, etc. Battery and solar-cell

operation requires an operating voltage environment in low voltage area. These conditions demand new design approaches and more sophisticated concepts to retain high device reliability. The proposed techniques (HSVR and GSVE) are topology based and hence easier to implement. The substantial reduction in leakage currents obtained proves them to be as effective as any fabrication level technique would be.

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