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Wide Range Frequency Synthesizer using Variable Length Ring Oscillator

H. Mondal[1] and M. K. Mandal[2,*]

[1]Department of Physics, Durgapur Govt. College, Durgapur - 713214, West Bengal, India.

[2]Department of Physics, National Institute of Technology, Durgapur – 713209, West Bengal, India.

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ABSTRACT

In this paper, we have presented a wide range phase locked loop (PLL) based frequency synthesizer using a voltage tuning variable length ring oscillator (RO). The frequency of the used ring oscillator can be changed dynamically from one frequency to another frequency by changing the length of the oscillator electronically. An analog frequency tuning mechanism is also introduced here to make it suitable for applications in PLL based systems. The proposed PLL based frequency synthesizer can successfully synthesize different harmonics (Nf_r) of the reference signal (f_r) within the lock range of the oscillator. The experimental results from a prototype hardware electronic circuit are presented here to support the validity of the proposed architecture of the RO and the frequency synthesizer.

Introduction

Wireless communication systems have grown tremendously in the past one and half decades due to the availability of portable electronic transceiver. The performance of such communication transceiver heavily depends on the frequency synthesizer, i.e., frequency selecting component as well as synchronisable local oscillator used in the portable devices. The frequency synthesizer available in the literature can be classified into two groups: one is direct digital frequency synthesizer [1,2] and the other group is indirect PLL based frequency synthesizer (FS) [3-5]. Although the design of frequency synthesizer is an old age problem but till today the design of high performance and low cost frequency synthesizer is a challenging work to the system designer and researcher. The properties of an FS on which a designer is interested are (i) larger frequency range of the synthesized signals, (ii) lower power consumption by the synthesizer, (iii) better spectral purity of synthesized signals, (iv) ease and speed of frequency switching from one value to the other, (v) resolution of synthesized frequencies etc. PLL based frequency synthesizer use frequency divider as one of constituent sub-circuit, which scales down the frequency of the loop oscillator to the frequency of the reference signal (f_r). The frequency of the synthesized signal (f_s) is changed by changing the division factor (N) of the divider since $f_s = Nf_r$ at the locked condition of loop operation. However, the divider circuit designed using digital flip-flops have some demerits in the overall performance of the frequency synthesizer. The key component of a frequency synthesizer is its local oscillator because the performance of the synthesizer heavily depends on its oscillator. There are many types of oscillators like, harmonic oscillator [6], relaxation oscillator [7], ring oscillator [8], etc. can be used as voltage controlled oscillator (VCO) in PLL for different applications. In this article we have focused our attention on ring oscillator based frequency synthesizer because ring oscillator have the benefit of being small size, easy to design, high oscillation frequency with dissipating low power and offer a wide tuning range.

The rest of the paper is organized in the following way. The structure and operation of the frequency synthesizer is described in section 2 with giving emphasis on the structure and operation of variable length ring oscillator. Experimental results and discussion are given in section 3. The outcomes of the whole study are summarized in the conclusion section.

Structure and operation of FS

The structure of the proposed frequency synthesizer circuit is shown in Fig. 1. The main functional blocks used in this circuit are phase frequency detector (PFD), charge pump low pass filter (CP-LPF), voltage controlled variable length ring oscillator (VC-VLRO) and a frequency divider (FD). The purpose of the frequency divider is to divide the output signal frequency of the VC-VLRO in such a way that it maintains $f_s = Nf_r$. The structure and operating principal of PFD, CP-LPF and VC-VLRO are described in the following subsections.

Phase frequency detector

The phase frequency detector has been implemented with digital sequential circuits and can detect both phase and frequency. Figure 2 shows the structure of PFD along with the conceptual timing diagrams of its input and output waveforms under open loop conditions. The outputs of the PFD are two digital control signals called UP and DOWN. If the oscillator signal (V) leads the input reference signal, implying that the VC-VLRO has to slow down a bit, the DOWN signal will be activated. When the VC-VLRO signal is lagging the input reference signal (which means the VC-VLRO has to speed up), the UP signal will be activated. The advantage of this PFD is that neither the UP nor the DOWN signal is activated when the PLL is in a locked condition. This state is known as NULL. So, the PFD has three possible logic states at their output terminal for which they are known as 'tri-state'. The states are commonly designated as U, D and N. The width of the pulses in U or in D will be the same when input reference signal and oscillator signal are in same frequency, but if their frequencies are different then the width of the pulses in U or in D will be different. The duration of pulse width in U or in D is determined

Tele:

E-mail addresses: mrinalkanti.mandal@phy.nitdgp.ac.in

by the magnitude of the phase error between input reference signal and oscillator signal.

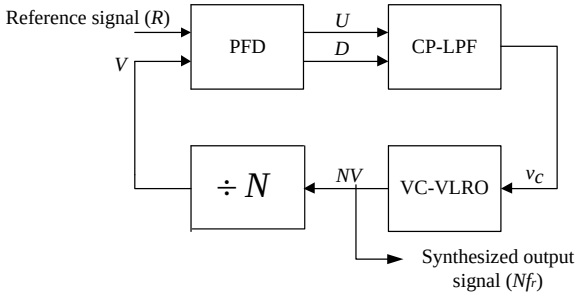

Figure 1. Block diagram of the proposed frequency synthesizer.

Charge pump low pass filter

The charge pump circuit converts the logic states of *U* and *D* into currents, which can have three values *Ip* (*U* is high), *-Ip* (*D* is high), and 0 (*U* and *D* are low). The duration of the pump current is proportional to the phase difference between the signals *R* and *V*.

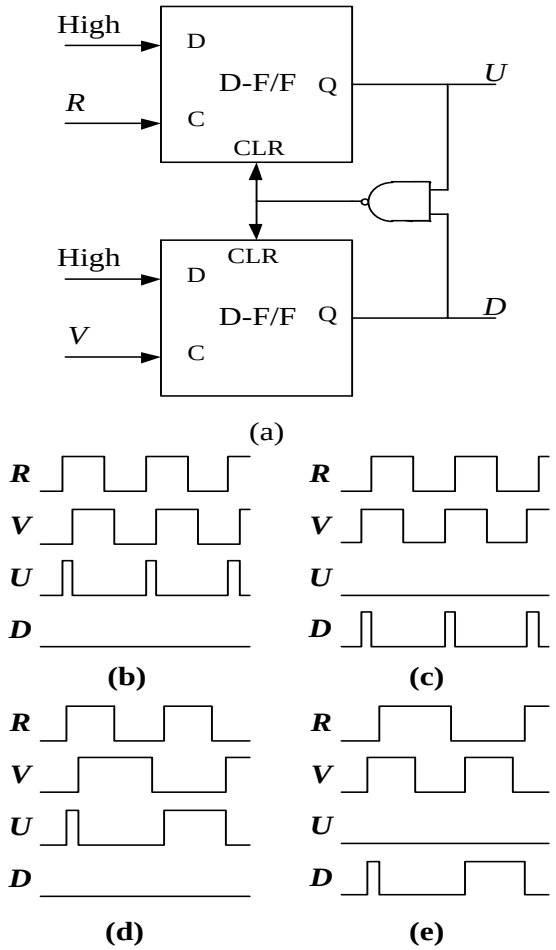

Figure 2. Structure and timing diagram of input signals and output signals of the PFD: (a) PFD structure, (b)*R* leads *V*, both are at the same frequency, (c)*V* leads *R*, both are at the same frequency, (d)*R* leads *V* and they are at different frequencies, (e)*V* leads *R* and they are at different frequencies

The loop filter converts the pump current into an analog voltage, which is used to control the frequency of the VC-VLRO. The hardware structure of the CP-LPF circuit is shown in Fig.3. The operation of the circuit can be explained as follows. When *U* and *D* are both low, the transistors *Q3* and *Q4* are in cut-off state and the R-C network will provide fixed v_c. When *U* is in high state and *D* is in low state, *Q3* draws current *Ip* through the current mirror comprising of *Q1* and *Q2*; thus, *Ip* current goes into the R-C network through *Q2* (since *Q4* is cut off). Hence, v_c increases. Alternatively, when *D* is in high state and *U* is in low state, *Q3* is off but *Q4* conducts and draws a current *Ip* from R-C network. Hence, v_c would gradually decrease. This operation has been explained in Fig. 3.

Voltage controlled variable length ring oscillator

The basic ring oscillators consist of an odd number of inverters connected in a closed loop chain. The steady oscillation in a ring oscillator requires a total phase shift of 2π around the loop at a frequency where the small signal gain is about 0dB. In an *n*-stage ring oscillator, each stage contributes with a frequency dependent phase shift of π/n and the dc inversion provides the remaining phase shift of π. This means that for a ring oscillator with single ended inverter stages, an odd number of stages are necessary for the dc phase shift of π. Therefore the oscillating signal must go through each of the *n* delay stages once to provide the first π phase shift in a time of $n\tau_d$ and it must go each stage a second time to obtain the remaining π phase shift in a time period of $2n\tau_d$. Thus the frequency of oscillation will be $f_{osc} = 1/2n\tau_d$. Since the oscillation frequency is determined by the number of inverter stages (n) and by their propagation delays (τ_d), thus this configuration of RO does not allow for a change in frequencies. But the frequency of ring oscillators can be tuned by applying an analog control voltage to each node of the oscillators or by changing the length of the oscillator.

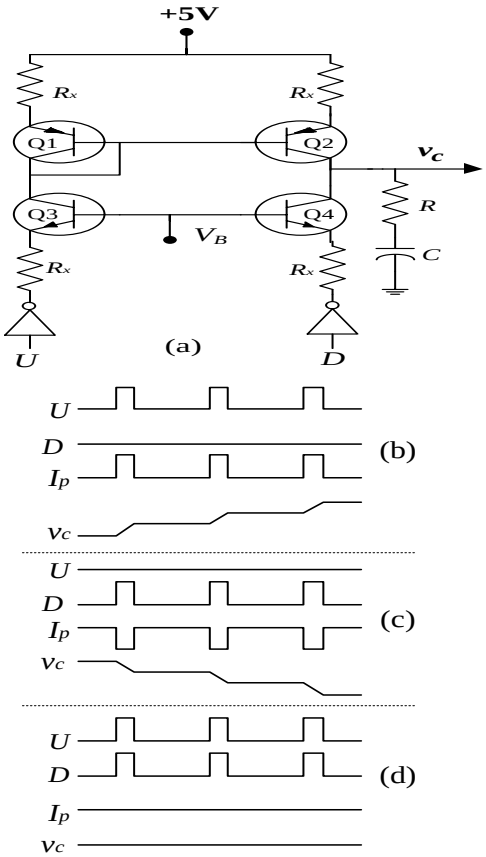

Figure 3. Structure and operation of CP-LPF: (a) Hardware structure of CP-LPF, (b) pump current and the low pass filter output when reference signal leads oscillator signal, (c) pump current and the low pass filter output when reference signal lags oscillator signal and (d) pump current and the low pass filter output when reference signal and oscillator signal are in phase.

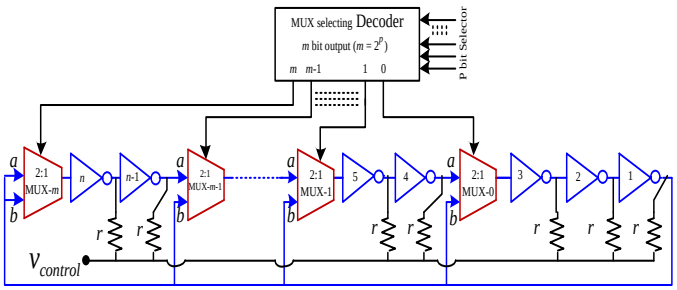

Figure 4. Proposed architecture of high speed VLRO with frequency tuning mechanism

An efficient variable length ring oscillator architecture [9] with voltage tuning mechanism is presented in Fig. 4. The oscillator consists of main three components: inverters, 2-to-1 MUXs and a decoder. The purpose of the decoder is to select a 2-to-1 MUX at a time through which the loop of the ring oscillator is completed. Decoder outputs are connected to the control input of the 2-to-1 MUX. The output of the decoder, i.e., MUX control signal has only two states high or low. The high control signal of the MUX select *a*-input to its output and for low control signal it select *b*-input as indicated in Fig. 6. Thus the ring is completed through a particular MUX whose control signal is low. For example, if control of MUX-0 is low then the loop is completed through first three inverters and MUX-0, if control of MUX-*m* is low then the loop is completed through all the inverters and MUXs. A suitable *p*-bit selection word is used in the decoder for the above purpose. On the other hand, all the outputs of the inverters are connected to the control dc voltage through suitable resistance. By controlling the dc voltage, the oscillating frequency of the oscillator can be tuned within a specified range of frequency. The frequency of this ring oscillator can be tuned by two ways: one is course tuning can be done changing the length of the ring structure with the help of *p*-bit selection word of the decoder and another one is fine tuning can be done by changing control dc voltage. For generalized case we consider total n number of inverters (n is odd number) and $N = m + 1$ number of 2-to-1 MUXs are present in the loop. Thus the relationship between inverter and MUX number is $= (n - 1)/2$. Therefore the frequency of oscillation of this ring oscillator is given by

$$f_{osc-VLRO} = \frac{1}{2\left[n\tau_d + \left(\frac{n-1}{2}\right)\tau_m\right]} \quad (1)$$

Experimental results

The proposed frequency synthesizer circuit has been designed using commercially available ICs (D-F/F: 7474, NAND gate: 7400, open collector inverter: 7406, MUX: 74257, decoder: 74154 and divider 74193) and other electronic circuit components like transistors (BC547 and BC548) capacitors and registers. In this experiment a thirty three stages variable length ring oscillator based on multiplexer and decoder has been designed to use as a voltage controlled oscillator (VCO) in the PLL based frequency synthesizer. The variation of frequency of oscillation of the oscillator with the number of stages is shown in Fig. 5. In this figure the points are experimental data and the solid line is the best matched curve according to equation (1) to the data using ORIGIN software. The constant values of τ_d and τ_m of equation (1) calculated from this software are 14.9 and 8.4 nanosecond respectively. The variation of oscillation frequency with control voltage for different ring length (different number of inverters in the oscillator chain) is shown in Fig. 6.The performance of the proposed frequency synthesizer has been tested through the hardware circuit and we have observed different harmonics for different division factor. The reference frequency used in the synthesizer is $f_r = 160KHz$ from a function generator. The synthesized 8th and 16th harmonics of the reference signal are shown in Figs. 7 and 8 respectively. Figure 7(a) shows the spectrum of the synthesized signal for $N = 8$ (number of inverter in the ring oscillator is 21) and Fig. 7(b) shows its time domain representation (upper waveform is reference signal and lower waveform is the required synthesized waveform). Similarly, Fig. 8(a) and (b) shows the frequency spectrum and time domain representation of the synthesized signal for $N = 16$ (number of inverter in the ring oscillator is 15) respectively.

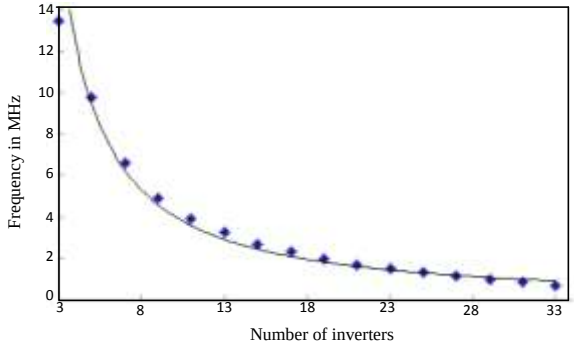

Figure 5. The variation of oscillation frequencies with the number of inverters for constant control voltage of 2.5 volt

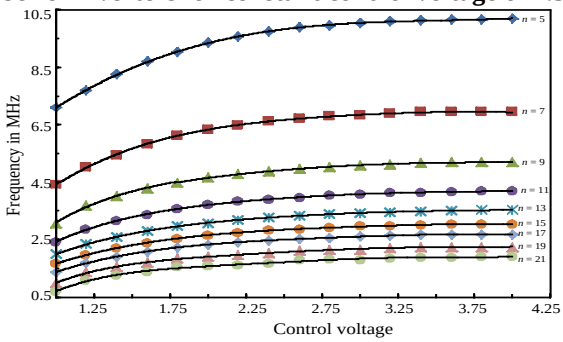

Figure 6. The variation of oscillation frequencies with the control voltage for different values of n

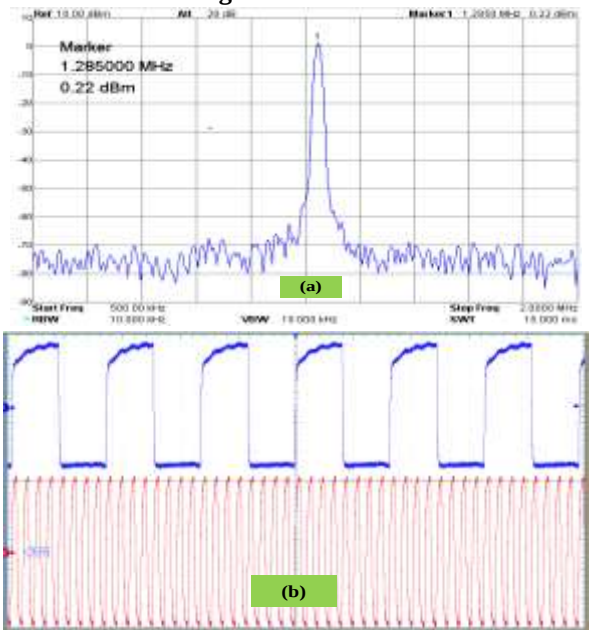

Figure 7. The synthesized signal for $N = 8$: (a) frequency spectrum and (b) synthesized waveform (lower tracing), reference signal (upper tracing); x-axis: 3.85μs/div. y-axis: 1V/div

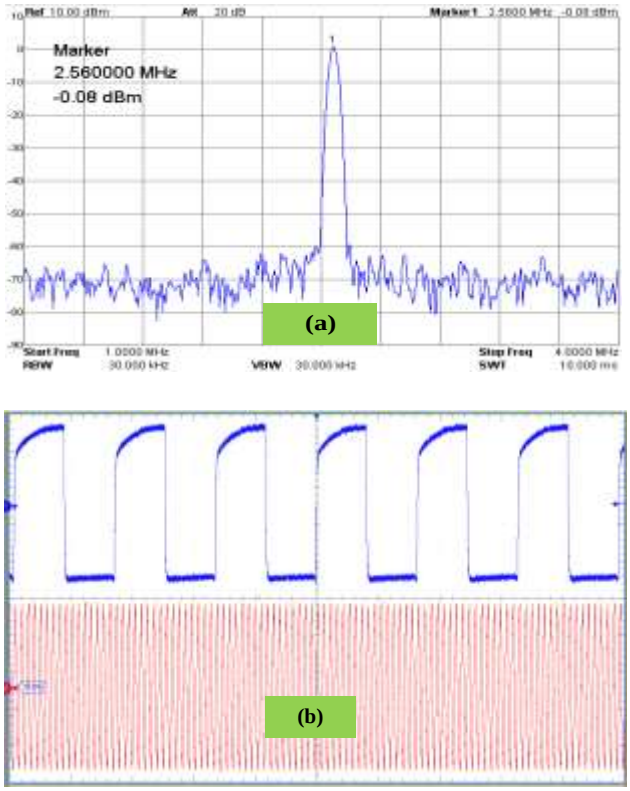

Figure 8. The synthesized signal for $N = 16$: (a) frequency spectrum and (b) synthesized waveform (lower tracing), reference signal (upper tracing); x-axis: 3.85µs/div. y-axis: 1V/div.

Conclusions

We have described and designed variable length ring oscillator for clock signal synthesis for many applications in communication. The proposed variable length ring oscillator has two mechanisms for frequency control: i) Fine control- by changing control voltage, ii) Coarse control- by changing MUX selection word through decoder (length control). So, this type of oscillator is suitable for PLL based communication transceiver design. One useful application of this oscillator in PLL based frequency synthesizer is also successfully presented here. The synthesized signal obtained from the synthesizer are present in the lower end of the RF spectrum but it is possible to design the proposed circuit monolithically in IC to get the synthesized frequency in the higher region of the frequency spectrum.

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References

H. C.Yeoh, J. H.Jung, Y. HJung and K. H. Baek, "A 1.3-GHz 350-mW hybrid direct digital frequency synthesizer in 90-nm CMOS", *IEEE J. Solid-State Circuits*, vol. 45, pp. 1845-1855, September 2010.

B. C. Sarkar and M. K. Mandal, "Ring oscillator based direct digital frequency synthesizer with improved spectral purity", *Indian J. Pure and Applied Physics*, vol. 41, PP. 402-407, May 2003.

A. Maxim, et. al., "A fully integrated 0.13-µm CMOS digital low-IF DBS satellite tuner using a ring oscillator-based frequency synthesizer", *IEEE J. Solid-State Circuits*, vol. 42, pp. 967-982, May 2007.

A. Jakobsson, C. Grewing, A. Serban and S. Gong, "Frequency synthesizer with dual loop frequency and gain calibration", *IEEE Trans. Circuits and Systems-I*, vol. 60, pp. 2911-2919, November 2013.

S. Min, T. Copani, S. Kiaei and B. Bakkaloglu, "A 90-nm CMOS 5-GHz ring-oscillator PLL with delay-discriminator-based active phase-noise cancellation", *IEEE J. Solid-State Circuits*, vol. 48, pp. 1151–1160, May 2013.

H.Ransijnand P. O'Connor, "A PLL-based 2.5 Gb/s GaAsclockand data regenerator IC", *IEEE J. Solid-State Circuits*, vol. 26, pp.1345–1353, October 1991.

M. Souyer and H. A. Ainspan, "A monolithic 2.3Gb/s 100mW clock and data recovery circuit", *IEEE Int. Conf. on Solid-State Circuits and systems*, pp. 158–159, 1993.

S. K. Enam and A. A. Abidi, "A 300MHz CMOS voltage-controlled ring oscillator", *IEEE J. Solid-State Circuits*, vol. 25, pp. 312–315, January 1990.

M. K. Mandal and H. Mondal, "Design of variable length ring oscillator for clock synthesis", *Int. Conf. on Information Technology in Signal and Image Processing*, pp. 271-275, Oct. 18-19, 2013, Mumbai, India.