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# Semiconductor device noise and impact on high speed communication circuits

P. K. Talam, R.K. Kosgei* and S.E.O.Obota

Department of Physical Sciences, University of Kabianga, P.O. Box 2030-20200, Kericho, Kenya.

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**ABSTRACT**

Noise is defined as any unintended signal that interferes with circuit operation. Although this includes spurious signals of human origin or the external environment, this investigation is limited to noise that result from microscopic fluctuations within the semi-conductor components of the circuit. While noise is typically seen as an analog circuits problem, it is believed that noise will become of greater concern in digital circuits as devices shrink, power supply voltages are reduced, and the number of carriers conducted by these devices is reduced. Noise under large-signal conditions is an important consideration in the design of wireless communications circuits. It has an effect on the spectral purity of oscillators and the noise figure of mixers and power amplifiers. The ability to simulate the noise of LC Voltage- Controlled Oscillators (VCOs) makes it possible to predict their performance in these types of circuits. It is then possible to have a better picture of the worst-case performance of these circuits so that overdesign or costly redesigns are not necessary. This paper presents the development and simulation techniques and mathematically accurate models at the component level resulting in optimization of *low frequency loading, feedback circuit and emitter degeneration* which can help minimize the phase noise in FET oscillators subject to design constraints such as power dissipation, tank amplitude, tuning range, start-up condition, and diameter of spiral inductors.VCO output frequency is tuned by on-chip p /n-well junction varactors. The circuit topology minimizes the amount of fixed parasitic capacitance in the tank circuit. The simulation results show that the proposed VCO can reach the frequency wished to the telecommunication application. Parameters from an industrial0.35 µm CMOS process are used for simulations. The nominal operating frequency of these oscillators is 2.4 GHz. They are designed to be resistant to supply and temperature effects. This oscillator achieves the necessary temperature and supply independence while being tunable about 2.4 GHz. Using only 2.5V of power supply and 1V of tuned voltage, the circuit shows a simulated single-output sensitivity of 565ppm/°C at 27C temperature and -0.47%/Volt at 2V.



## Introduction

Noise is an important consideration in the design of a communications circuit. The noise performance of a circuit determines the threshold for the minimum signal that can be applied at the input of the circuit and can be detected at the output. This translates into how accurately a signal can be transmitted and then be received. Although wireless communication has become a digital medium, noise is still an important consideration because analog circuitry is still required for the transmission and reception of the desired information.

In nonlinear circuits, noise is dependent on the large-signal currents flowing through the semiconductor devices (K. Mayaram et al, 2000). In this work we address the problem of designing the best LC tank for radiofrequency applications (P.Andreani, et al, 2000). Due to the ever-increasing demand for bandwidth, very stringent requirements are placed on the spectral purity of local oscillators. Efforts to improve the phase-noise performance of integrated *LC* VCOs have resulted in a large number of realizations (N. M. Nguyen et al, 1992). Despite these endeavors, designand optimization of integrated *LC* VCOs still pose many challenges to circuit designers as simultaneous optimization of multiple variables is required. A computer-aided optimization technique using *geometric programming* has been recently used to find the optimum design for certain *LC* oscillator topologies efficiently (M. Herschensohn et al, 1999). Despite its efficiency, it provides limited insight into the underlying tradeoffs among the many design parameters which are essential to enhance circuit innovations and increase design productivity. Integration of high quality factor passive networks is difficult because of losses due to silicon substrate, capacitive and inductive parasitic. These effects are more important at high oscillation frequencies. In order to achieve high performance fully-integrated Q-VCO, high-Q inductors and varactor have been integrated on the VCO circuit (D. Ham et al, 2001).

## Circuit Theory

The CMOS oscillator circuit employs both NMOS and PMOS cross-coupled pairs. In a simple CMOS–$G_M$ oscillator the same bias current flows through both the NMOS and PMOS devices, consequently for the same power consumption the configuration yields a negative resistance twice as large. The total negative resistance of the CMOS pair can be expressed as a

Tele:

E-mail addresses: richardkosgei1@yahoo.com

parallel combination of the NMOS and PMOS pair's negative resistance, $R_{inn}$and $R_{inp}$,as:

$$R_{negative} = R_{inn} // R_{inp} = -\frac{2}{G_{mn} + G_{mp}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

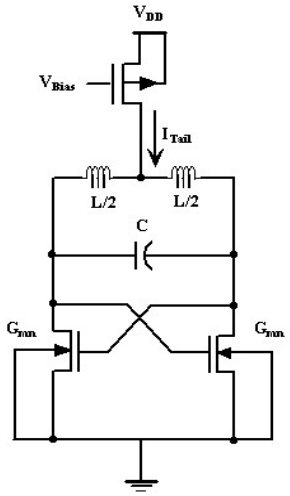



**Figure.1. NMOS-only oscillatorwith a tail current source (J. Craninckx, 1997).**

The CMOS differential topology is accompanied by a fair share of drawbacks characteristic of the configuration in use. An important difference between the complementary -*GM* oscillator and its NMOS or PMOS only counterparts is in limiting the differential voltage swing. In complementary oscillators, the voltage swing is essentially limited by the supply voltage and the bias current, while, in NMOS or PMOS-only versions, solely by the bias current. NMOS or PMOS only circuits exhibit AC voltages wings that exceed *VDD*; however in complementary oscillators such voltage sojourns are limited by PMOS transistors driven into cutoff, restricting the bias current to NMOS devices. Also, the use of more than two active devices other than only the NMOS or PMOSpairs increases the number of noise sources and the parasitics, thereby resulting in detrimental effects on the phase noise and frequency performance tuning characteristics.

**LC-VCO circuit descriptions and optimization**

**Use of emitter degeneration**

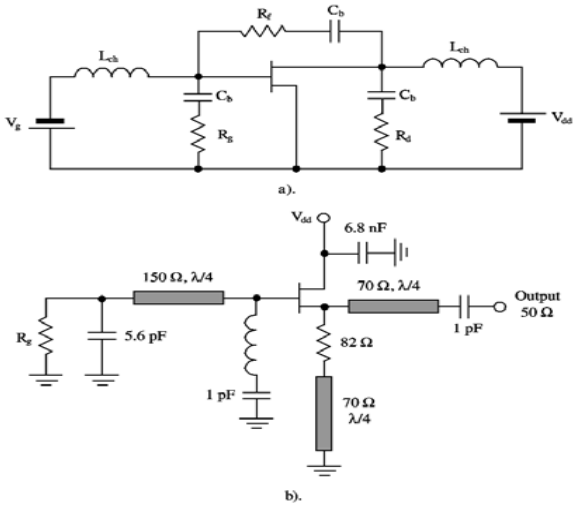


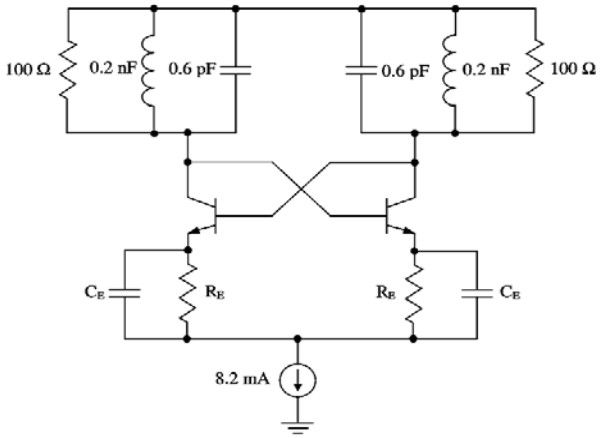

**Fig.2.Diagram of a low frequency circuit reducing phase noise**

In a first approximation, agate voltage noise generator connected in series with a noise-free nonlinear two-port circuit can model the low frequency phase noise in FET devices. So, if the low frequency voltages applied to gate-source and drain-source terminals are reduced, the resulting sideband components around the oscillation frequency dueto nonlinear mixing of these voltages will be reduced as well. To realize such an approach, it is necessary to provide the short circuiting of the drain port and open-circuiting of the gate port at low frequencies (M. Prigent et al, 1987). The phase noise improvement under these conditions was verified experimentally by connecting external variable resistances $R_g$ and $R_d$ to the gate and drain ports, as shown in Figure 1(a),where $C_b$are the blocking capacitances. The minimum phase noise conditions are realized for ideal case when $R_g = \infty$ and $R_d = 0$. This means that, in practice, a high value of external resistance $R_g$at low frequencies is needed when it is bypassed by the choke inductance $L_c$ and no converted noise variations will be observed.

It was found that 1/*f* noise could be approximated by a quasi-stationary phenomenon having a quasi-constant autocorrelation function (M. S. Keshner,et al,1982). Consequently, it is possible to reducephase noise by applying a feedback voltage in series with the 1/*f* noise generator using parallel resistor $R_f$ shown in Figure 2(a). The higher voltage gain from input to output, the stronger feedback may be applied and the lower variations of the gate-source voltage can be observed. The low frequency feedback circuit is also capable of canceling thermal noise at low frequencies. The amount of cancellation is determined by the circuit delay and the frequency. Due to gate and drain loading, an 8 dB phase noise improvement can be obtained at 1kHz offset from the carrier for 10 GHz micro wave oscillator. Optimizing the values of the gate, drain and feedback resistances results in overall 11 dB phase noise improvement with optimum values of $R_f = 0$, $R_g > 100\Omega$ and $R_d < 100\ \Omega$(M. Prigent,et al,1987).Figure 2(b) shows the circuit schematic ofa common drain microwave MESFET oscillator with a direct current resistor $R_g$ between the gate and the ground(A. N. Riddle,et al,1984). This low-frequency resistor, bypassed at high frequencies, also affects the noise up conversion by allowing the gate rectification current to produce an optimum reverse bias on the gate. The lowest phase noise was obtained when a gate resistor $R_g$=1 kΩ was used in the 5.6 GHz oscillator and a gate resistor $R_g$= 200 kΩ was used in the 7.4 GHz oscillator providing a14 dB noise reduction. Thus, there is an optimum value of the bias voltage minimizing the oscillator phase noise. In order to obtain low phase noise at low offset frequencies with dominating 1/*f* noise, the bias point should be chosen to avoid the increasing output conductance at the transition between the active and saturation regions, as well as operation in the pinch-off region should be minimized corresponding to a Class AB mode with high quiescent current (V. Gunderich et al, 1994). Within these limitations, it is necessary to maximize the oscillator output power. To keep the MESFET device operating in active region, the technique utilizing a pair of limiting diodes can be used (. A. M. Darwish et al, 1992). Two limiting diodes are placed between the source of the MESFET device and resonator to clip the oscillation amplitude before driving the transistor into nonlinear operation. Although adding a pair of diodes introduces new nonlinearities in the circuit, overall 1/*f* noise will be reduced since the MESFET is operated in a linear active region and the diode nonlinearities are small compared with those of the MESFET device.

Figure.2.shows a typical LC oscillator circuit based on a cross-coupled transistor pair incorporating emitter degeneration

(J.-H. C. Zhan,et al,2003).The proper choice of the parameters ofthe oscillation circuit provides the tuning range from 12to 15 GHz using bipolar devices with transition frequency $f_T$= 45 GHz from SiGe 6HP process. The oscillator phase noise at 2 MHz

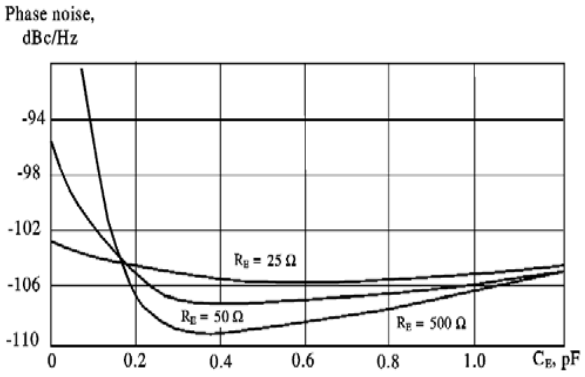



offset is illustrated in Figure 3.

**Figure.3.VCO topology incorporating emitter degeneration**

If degeneration capacitance $C_E$is too small; the noise generated by the feedback resistance $R_E$is not adequately filtered resulting in noise degradation. For a degenerated VCO with $R_E$= 300 Ω, varying capacitance $C_E$ from 0.3 to0.8 pF provides a tuning range of the oscillation frequency from 14.6 to 12.6 GHz. The optimum combination of the values of the degeneration resistance $R_E$ and capacitance $C_E$ improves the phase noise performance by approximately 7 dB compared with the non-degenerated design.

**Fig.4.Simulated phase noise of LC oscillator withemitter degeneration.**




**Use of Complementary transistors**

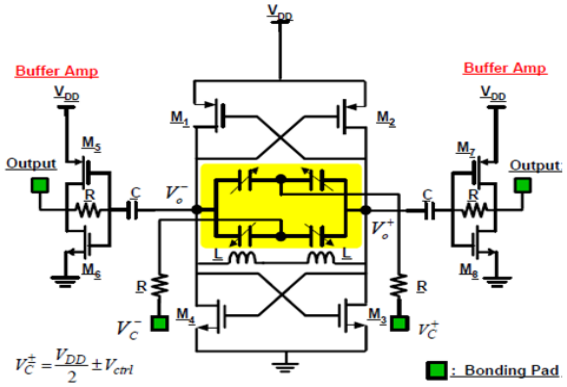



**Figure 5: Schematic of a typical VCO with differential outputs.**

Figure 5 shows a complementary oscillator. This–$G_M$ oscillator circuit is the result of using both PMOS and NMOS cross coupled pairs in parallel to generate the negative resistance**.** The circuit topology chosen for the LC oscillator was adapted from (Jing-Hong et al, 2002) and is shown in Figure 5. The cross-coupled NMOS devices (M3 and M4) form the negative resistance and the PMOS devices (M1 and M2) create a positive feedback load. M5 and M6 are perhaps the most important elements of the LC oscillator circuit besides the inductor itself.

There are several reasons for the advantage of the complementary structure used as the core circuit of the VCO. The complementary structure offers higher trans conductance for a given current, which results in faster switching of cross-coupled differential pair. It also offers better rise and fall-time symmetry, which results in less up conversion of 1/*f* noise and other low frequency noise sources (A. Hajimiri et al, 1999).In this oscillator, we use the process minimum channel length of 0.25µm and choose the appropriate channel widths to make the trans conductance of NMOS equal to the trans conductance of PMOS. Therefore, the dc level of the drain nodes in the complementary cross-coupled pair can maintain VDD/2 in order to achieve a more symmetric waveform. The source voltage of $M_1$, $M_2$, $M_3$ and $M_4$is directly connected at 0V and VDD (2.5V), respectively, without any extra current source. For low supply voltage operation, to enlarge the voltage swing by removing the use of current source, which reduces the voltage headroom, is one of the most direct ways to improve the phase noise performance. This bias scheme maximizes the oscillator signal peak-to-peak amplitude. The series combination of the two on-chip inductors constitutes the tank inductor. Because of the layout of the used inductor is asymmetric. Two inductors in series, placed in a vertical symmetric way, ensure that the same structure could be seen by the drain nodes of the cross-couple pair. This will result in a more symmetric waveform between two drain nodes. In this design, one side of the MOS varactor connects directly to the drain node of the cross-coupled pair, whose dc level is VDD/2, and the other is connects to positive ($V_c^+$) or negative ($V_c^-$) control voltage.

**Table 1. Summary of simulated results**

| Voltage (V) | 0 | 0.2 | 0.4 | 0.6 | 0.8 | 1 | 1.2 | 1.4 | 1.6 | 1.8 | 2.0 | 2.2 | 2.4 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Freq(GHz) | 2.3 | 2.3 | 2.3 | 2.3 | 2.3 | 2.4 | 2.4 | 2.5 | 2.4 | 2.3 | 2.3 | 2.3 | 2.3 |

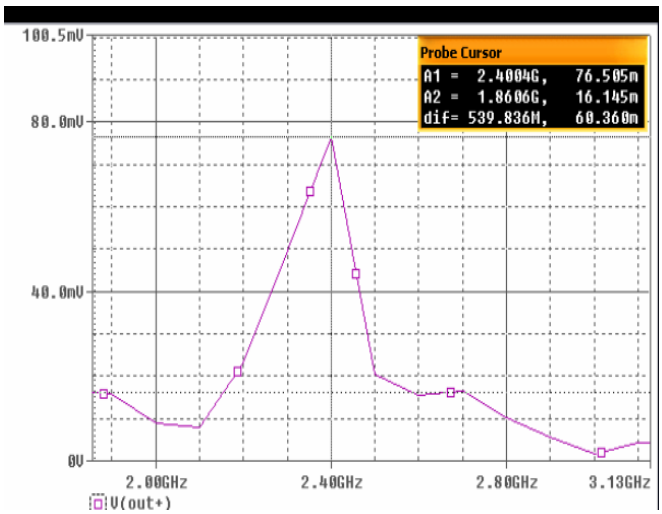



**Figure.6.Frequency spectrum of LC oscillator**

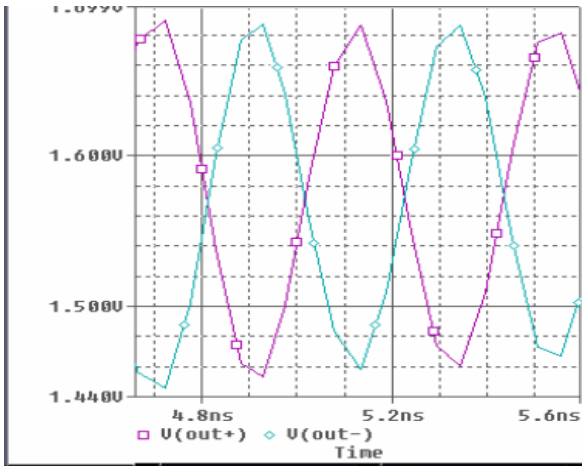



**Figure 7. Output waveform of LC oscillator**

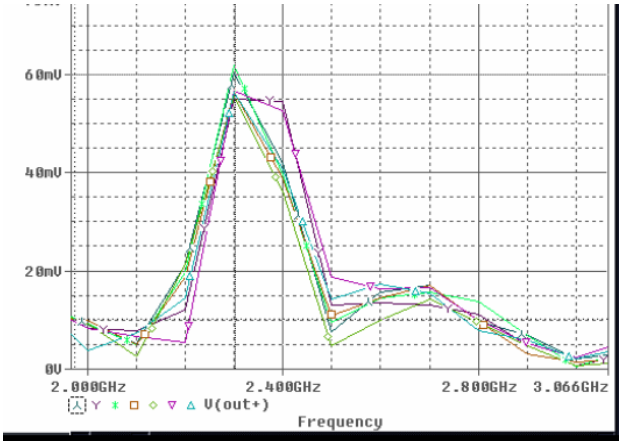



**Figure 8: VCO output spectrums for different value of temperature**

## Conclusion

From an intuitive viewpoint, this paper analyzes the oscillation frequency, tuning range and sensitivity of a fully integrated LC VCO fabricated in a 0.35-µm standard CMOS process. Design equations are provided that give reasonable prediction of circuit performance as verified by simulation. Using a voltage sweep of 2-3 V supply simulation at 2.4 GHz oscillation frequency, simple circuit scheme, and satisfactory sensitivity performance. VCO output frequency is tuned by on-chip p /n- well junction varactors.

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