Available online at www.elixirpublishers.com (Elixir International Journal)

Electronics Engineering

Elixir Elec. Engg. 72 (2014) 25392-25396

ISSN: 2229-712X

Design of efficient reversible multiplier using reversible gate

P.Arun* and P. Suresh Kumar

Deportment of ECE, Arunai Engineering College, Tiruvannamalai, India.

ARTICLE INFO

Article history:

Received: 16 May 2014;

Received in revised form:

20 June 2014;

Accepted: 1 July 2014;

Keywords

Garbage output,

Constant input,

Power consumption,

Gate count.

ABSTRACT

Multiplier is a basic arithmetic cell in computer arithmetic units. The energy consumption in computation turns out to be deeply linked to the reversibility of the computation. The primary objective of this paper was to gain insight into the Reversible Computation and its use for making circuits energy efficient for long life. In the recent years, reversible logic has emerged as a promising technology having its applications in low power CMOS, quantum computing, nanotechnology, and optical computing. In the proposed work, we synthesized a parity preserving reversible multiplier circuit with the help of existing fault tolerant Toffoli gate and SCG gate. Here partial products are generated using Toffoli gate and final sum is carry out using SCG gate. The proposed design is best compared to existing in terms of garbage output, constant input, power consumption.

Introduction

Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. Quantum computers are constructed using reversible logic circuits. It has wide applications in low power CMOS and Optical information processing, DNA computing, quantum computation and nanotechnology. In 1960 R.Landauer demonstrated that high technology circuits and systems constructed using irreversible hardware result in energy dissipation due to information loss [1]. According to Landauer's principle, the loss of one bit of information dissipates KTln2 joules of energy where K is the Boltzmann's constant and T is the absolute temperature at which the operation is performed [1]. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components. In 1973, Bennett, showed that one can avoid KTln2 joules of energy dissipation constructing circuits using reversible logic gates.

Reversible logic gates

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-out is not allowed as one–to-many concept is not reversible. However fanout in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits

(1)The number of Reversible gates (N): The number of reversible gates used in circuit.

(2)The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.

(3)The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.

(4)Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.

(5)Gate levels (GL): This refers to the number of levels in the circuit which are required to realize the given logic functions.

Reduction of these parameters is the bulk of the work involved in designing a reversible circuit. In this paper, an improved design of reversible multiplier with respect to its previous counterparts is proposed. Multiplier circuits play an important role in computational operation using computers. There are many arithmetic operations which are performed, on a computer ALU, through the use of multipliers. Design and implementation of digital circuits using reversible logic has attracted popularity to gain entry into the future computing technology.

Basic Reversible Logic Gates

Feynman Gate: Figureure1 shows a 2*2 Feynman gate [6]. The input vector is I (A, B) and the output vector is O (P, Q). The outputs are defined by P=A, Q=A⊕B. Quantum cost of a Feynman gate is 1.

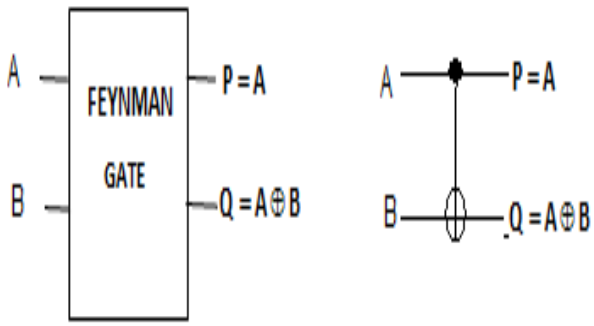

Figure 1. FEYMAN Gate

Double Feynman Gate (F2g):

Figure2 shows a 3*3 Double Feynman gate [7].The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P = A, Q=A⊕B, R=A⊕C. Quantum cost

Tele:

E-mail addresses: arun.tvr05@gmail.com

of double Feynman gate is 2.

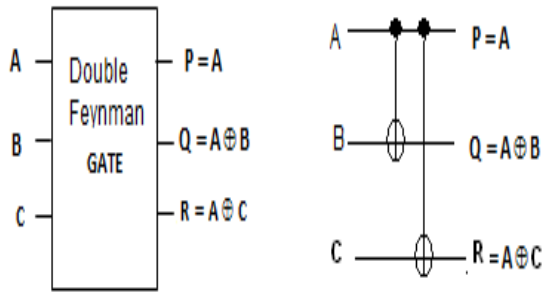

Figure 2. DFG Gate

Toffoli Gate:

Figure 3 shows a 3*3 Toffoli gate [3] The input vector is I(A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5.

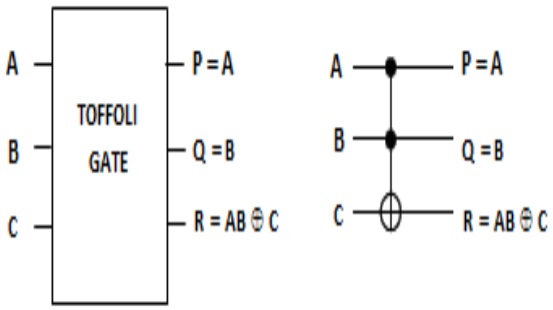

Figure 3. Toffoli Gate

Fredkin Gate:

Figure .4 shows a 3*3 Fredkin gate [4]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B⊕AC and R=A′C⊕AB. Quantum cost of a Fredkin gate is 5.

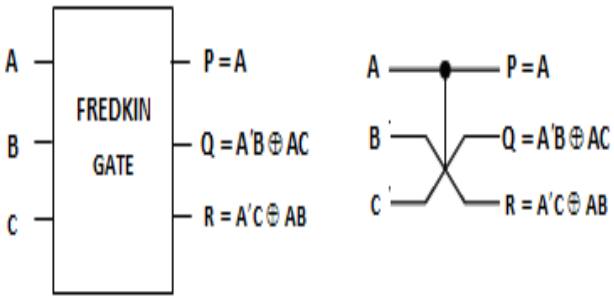

Figure 4. Fredkin Gate

New Gate (NG)

New gate (NG), is a 3x3 reversible gate. It can be represented as:

Iv = (A, B, C)

Ov = (P = A, Q = AB⊕C, R = A′C′⊕B′)

Where Iv and Ov are the input and output vectors. The New gate is shown in Figure. 2.5

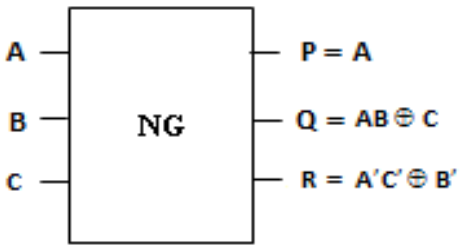

Figure 5. New Gate

TSG Gate

TSG gate is a 4×4 reversible gate. The TSG gate is shown in Figure.2.6, where each output is annotated with the corresponding logic expression:

Iv = (A, B, C, D)

Ov = (P = A, Q = A′C′ ⊕ B, R = (A′C′⊕ B′)⊕ D,

S = (A′C′⊕ B′) D ⊕ (AB⊕C))

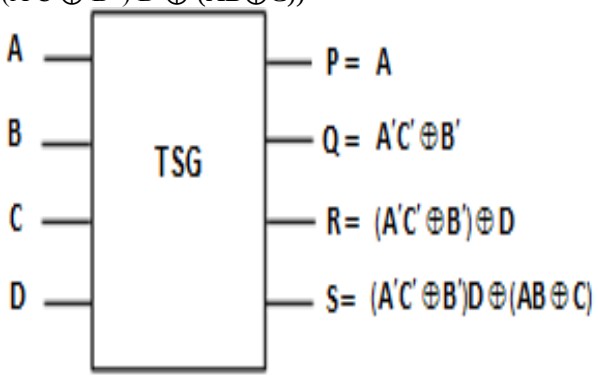

Figure 6. TSG gate

MKG Gate:

MKG gate is a 4x4 reversible logic gate. The MKG gate can be represented as:

Iv= (A, B, C, D)

Ov = (P = A, Q = C, R = (A′D′⊕B′)⊕C,

S = (A′D′⊕B′).C⊕(AB⊕D))

Where Iv and Ov are the input and output vectors.

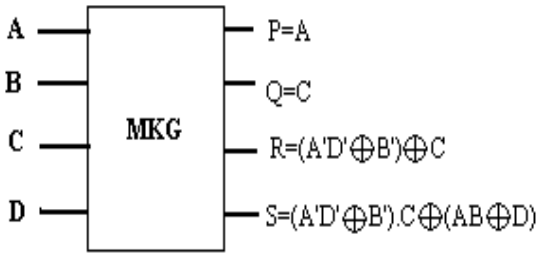

Figure 7. MKG gate

HNG Gate:

The HNG gate is universal. The HNG gate is shown in Figure.2.8., where each output is annotated with the corresponding logic expression. The corresponding logic expression of HNG gate:

Iv = (A, B, C, D)

Ov = (P = A, Q = B, R = A⊕B⊕C, S = (A⊕B).C⊕AB⊕D)

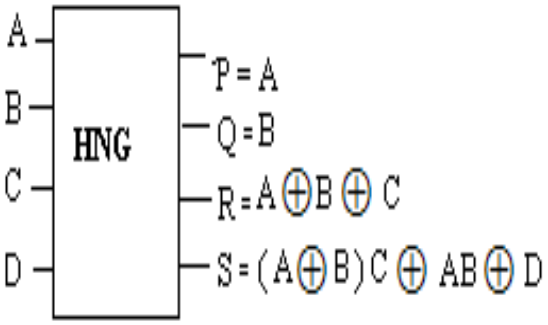

Figure 8. HNG gate

Proposed Design

Reversible Multiplier Design

A 4 * 4 reversible gate has been proposed in this paper (See Figureure3.1). The Truth table for the corresponding gate is shown in Table 1. A closer look at the Truth Table reveals that the input pattern corresponding to a specific output pattern can

be uniquely determined and thereby maintaining that there is a one-to-one correspondence between the input vector and the output vector. In this gate the input vector is given by $IV=(D,C,B,A)$ and the corresponding output vector is $OV=(P,Q,R,S)$. The inputs D,C,B and A are termed as the input terminals 1,2,3 and 4 respectively and the outputs P,Q,R and S are termed as the output terminals 1,2,3 and 4 respectively throughout the rest of the paper.

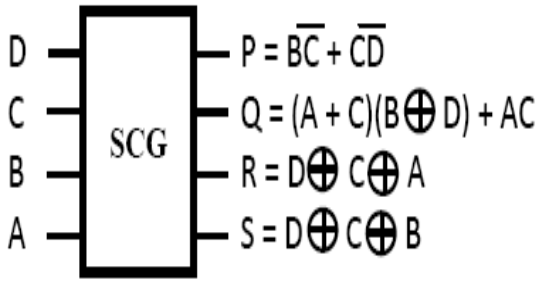

Figure 9. Proposed 4 * 4 Reversible SCG Gate

$$P = \sum m(2,3,4,5,6,7,10,11)$$

$$Q = \sum m(3,5,6,7,9,12,13,15)$$

$$R = \sum m(1,3,4,6,8,10,13,15)$$

$$S = \sum m(2,3,4,5,8,9,14,15)$$

D	C	B	A	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	1	0	0	1
0	0	1	1	1	1	1	1
0	1	0	0	1	0	1	1
0	1	0	1	1	1	0	1
0	1	1	0	1	1	1	0
0	1	1	1	1	1	0	0
1	0	0	0	0	0	1	1
1	0	0	1	0	1	0	1
1	0	1	0	1	0	1	0
1	0	1	1	1	0	0	0
1	1	0	0	0	1	0	0
1	1	0	1	0	1	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	1	1	1

Table 1. Truth table of Reversible SCG Gate.

Realizations of the Classical Operations

The proposed SCG gate can implement all the conventional boolean functions. Realization of AND operation, OR operation, XOR operation (See Figure10), NAND operation and XNOR operation (See Figure11), NOT operation, COPY operation (See Figureure3.4) are shown.

The fact that the proposed gate can implement NAND operation signifies that any boolean function can be implemented using the gate as NAND gate is a universal gate. Also since AND, OR and NOT operation can be implemented justifies the aforesaid because any boolean function can be materialized in product – of – sum or sum – of – products form. Also the COPY operation is an important operation which can be realized using the proposed reversible SCG gate.

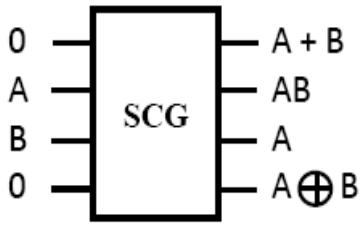

Figure 10: SCG gate implementing reversible AND, OR and XOR operation.

The configuration shown above can also be used in Carry Look Ahead Addition technique as $Gi= AiBi$ and $Pi= Ai+ Bi$ [18].

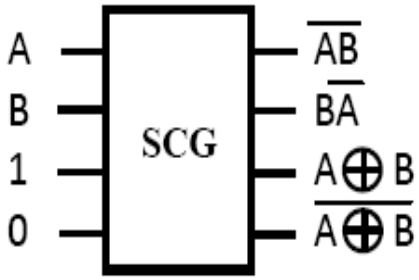

Figure 11: SCG Gate implementing reversible NAND and XNOR operation.

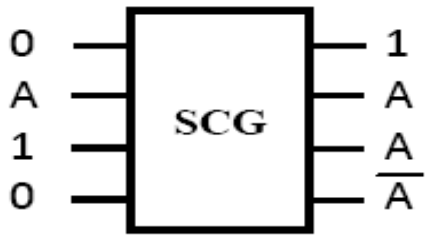

Figure 12: SCG Gate implementing reversible NOT and COPY operation.

In Figure 12, it can be seen that a signal A‟ is being produced at two output terminals, hence it can be said that the signal has been copied. Also the fourth output terminal produces the compliment of „A‟ thereby justifying the NOT operation.

Realizations of Parallel Adder/Subtractor

The most promising fact of the proposed SCG gate is that this gate can singly be used as a Full Adder as well as a Full Subtractor circuit with minimum amount of garbage outputs and constant inputs. Figure 13 shows the implementation of the SCG gate as a Full Adder and Figure 14 shows the implementation as a Full Subtractor. In Table 2, a detailed description of the number of reversible gates required and garbage outputs is given together with a comparison with other Reversible Full Adder/Subtractor designs in literature. Also in Table 2, a comparison has been done in the Reversible Comparator domain.

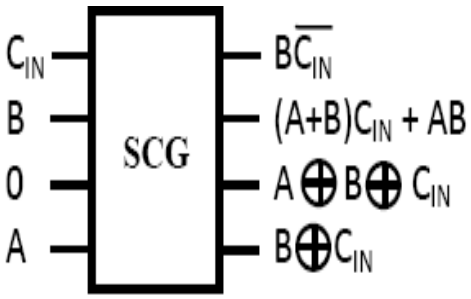

Figure13: Full Adder using a single Reversible SCG Gate

The second output terminal in Figure 14 corresponds to the Carry-Out and the third terminal the Sum output of a Full Adder. In Figure 3.6, again the second terminal on the output side of the reversible gate corresponds to the Borrow-Out and the third terminal the Difference output of a Full Subtractor.

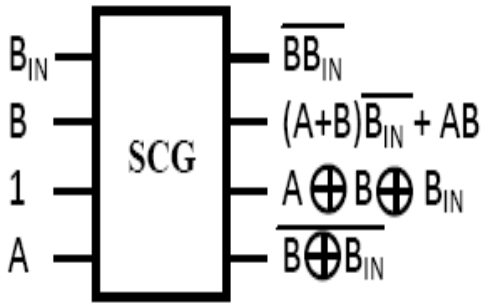

Figure14: Full Subtractor using a single Reversible SCG Gate

As a single SCG gate is enough for the implementation of a full Adder/Subtractor, hence an n – bit parallel Adder/Subtractor can be implemented using n SCG gates only.

Name of the gate	Full Adder / Subtractor		Number of gates required for Single Bit Comparator	Universal Gate NAND/NOR realization
	No. of gates	No. of garbage outputs		
SCG	1	2	1	1 gate
TSG [17]	1	2	More than 1	1 gate
HNG [16]	1	2	More than 1	1 gate
IG [19], [22]	2	3	More than 1	1 gate
Fredkin Gate [23]	5	4	More than 1	More than 1 gate
Feynman gate and New gate [20]	3	3	More than 1	Not Applicable
Feynman gate and Toffoli gate [20]	4	2	More than 1	Not Applicable
Feynman gate, New gate and Toffoli gate[20], [21]	3	2	More than 1	Not Applicable

Table 2. Comparative results on different Reversible Full Adder/Subtractor circuits

Reversible Multiplier Circuit

The operation of the 4x4 multiplier is depicted in Figure.4.1. It consists of 16 partial product bits of the form xi.yi. The proposed reversible 4x4 multiplier circuit has two parts. First, the partial products are generated in parallel using TOFFOLI gate.

The basic cell for such a multiplier is a full adder (FA) accepting three bits.Here SCG gate is used as full adder.

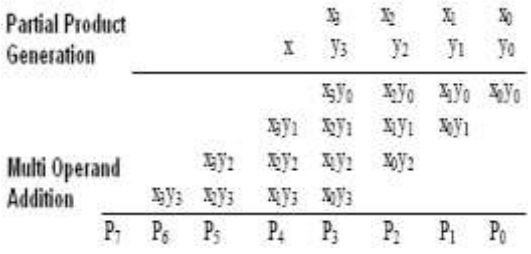

Figure 15. Multiplication

Partial Product Generation(PPG)

For product term generation the FRG gate is used. The TG gate is used to perform AND operation by forcing one constant input as logic 0 whereas it produces required product term along with two garbage outputs. The Figure. 15 shows the implementation of AND operation using TG. Figure. 16 TG as AND gate

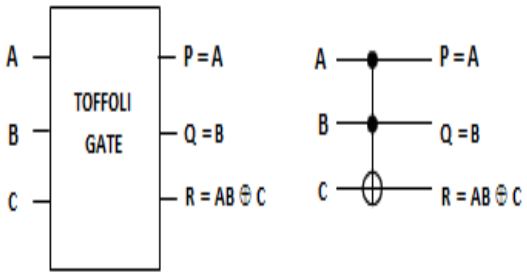

Figure 16 Toffoli gate

Multiplier partial products are generated in parallel using 16 Toffoli gate as shown in Figure.16 This uses 16 toffoli is a better circuit as it has less hardware complexity compared to other gates and moreover it posses parity preserving logic.

Figure 17 Partial product generation using Toffoli gate

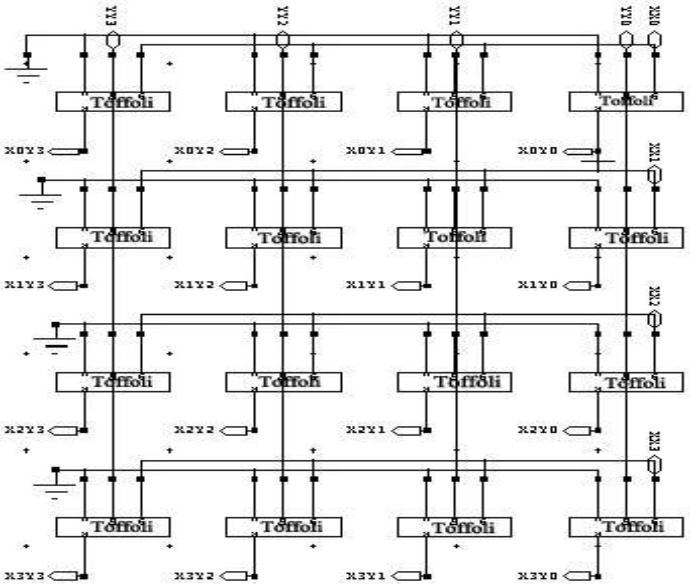

Figure 17: Partial product generation using Toffoli gate

Final Addition

Her SCG gate is used as a full adder. The overall architecture of the proposed multiplier design is as follows

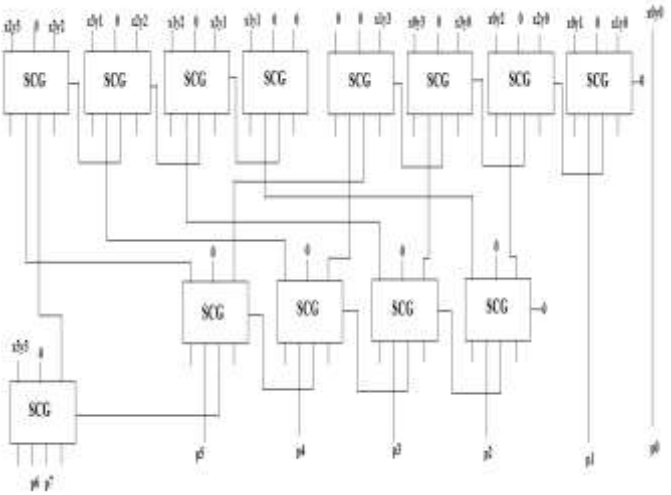

Figure 18. Overall architecture for 4*4 reversible multiplier.

Simulation Result

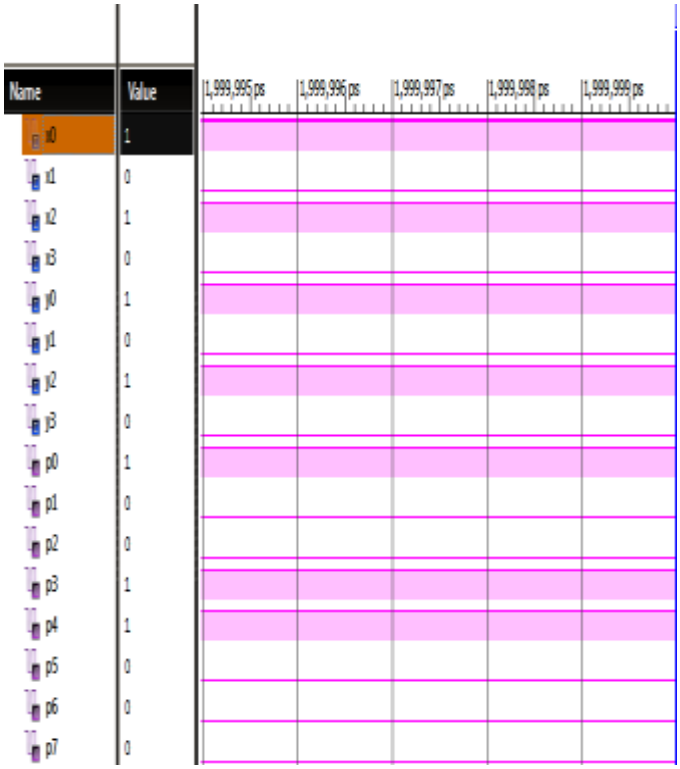

Figure 19. Simulation result for 4*4 multiplication

Device Utilization Summary

Device Utilization Summary			
Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	0	126,800	0%
Number of Slice LUTs	21	63,400	1%
Number used as logic	21	63,400	1%
Number using O6 output only	7		
Number using O5 output only	0		
Number using O5 and O6	14		
Number used as ROM	0		
Number used as Memory	0	19,000	0%
Number used exclusively as route-thrus	0		
Number of occupied Slices	13	15,850	1%
Number of LUT Flip Flop pairs used	21		
Number with an unused Flip Flop	21	21	100%
Number with an unused LUT	0	21	0%
Number of fully used LUT-FF pairs	0	21	0%
Number of slice register sites lost to control set restrictions	0	126,800	0%
Number of bonded IOBs	16	210	7%

Figure 20. Device Utillization

Applications

The reversible logic will have many applications. Some important areas of reversible logic include the following

✓Nanocomputing

✓Bio Molecular Computations

✓Laptop/Handheld/Wearable Computers

✓Spacecraft and Low power CMOS.

✓Design of low power arithmetic and data path for digital signal processing (DSP).

Power Dissipation

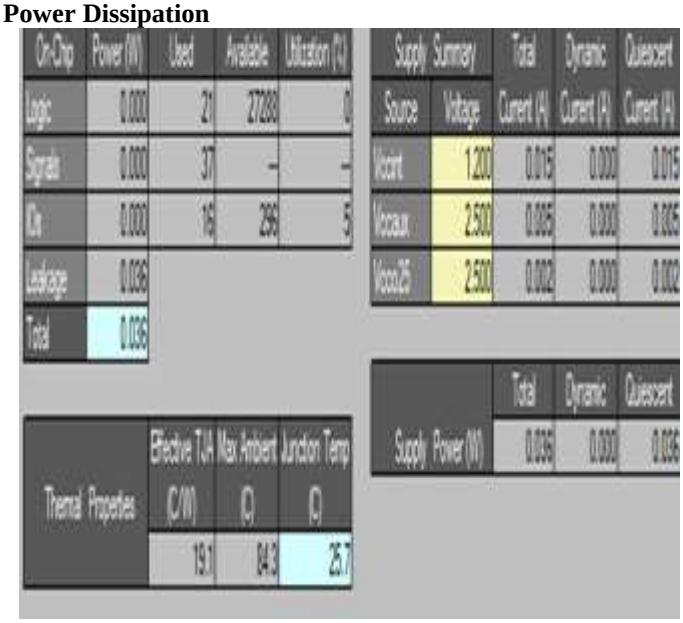

Figure 21. Power Analysis

Conclusion

The primary objective of this paper was to gain insight into the Reversible Computation and its use for making circuits energy efficient for long life Multiplier is a basic arithmetic cell in computer arithmetic units. The energy consumption in computation turns out to be deeply linked to the reversibility of the computation.. In the proposed work, we synthesized a parity preserving reversible multiplier circuit with the help of existing fault tolerant Toffoli and SCG gate. Thus, our proposed parity-preserving multiplier circuit can be used in designing fault tolerant reversible complex circuits like ALU. Using such circuit can be helpful not in terms of power saving but also acts as high speed multiplier for dedicated hardware. The prospect for further research includes the reversible implementation of more complex arithmetic circuits such as function evaluation and multiplicative division circuits using this multiplier.

References

[1] Landauer, R., "Irreversibility and heat generation in the computing process", *IBM J. Research and Development*, vol. 5 (3): pp. 183-191, 1961.

[2] M. P. Frank, "Introduction to reversible computing: motivation, progress and challenges", *In Proceedings of the 2nd Conference on Computing Frontiers,* 2005, pp 385-390.

[3] Bennett, C.H., "Logical reversibility of computation", *IBM J. Research and Development*, vol. 17: pp. 525-532, 1973

[4] Peres, A., "Reversible logic and quantum computers", Physical Review: A, vol. 32 (6): pp. 3266-3276, 1985.

[5] H Thapliyal and M. Srinivas, "Novel reversible TSG gate and its application for designing carry look ahead adder and other adder architectures", *Proceedings of the 10th Asia-Pacific Computer Systems Architecture Conference (ACSAC 05),* 2005, pp 775-786.

[6] G Schrom, "Ultra Low Power CMOS Technology", PhD Thesis, Technischen Universitat Wien, June 1998.

[7]M.S.Islam et al., "low Cost Quantum Realization Of Reversible Multiplier Circuit", Information Technology Journal, 8(2008)208.

[8] Bhagyalakshmi, H.R.;.Venkatesha, M.K, „An improved design of a multiplier using reversible logic gates", International Journal of Engineering Science and Technology Vol. 2(8), 2010, 3838-3845