



## Modified Sequential Switch Coding Technique for Low power dissipation in DSM Technology

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### ABSTRACT

The power dissipation in a system-level attributes to buses is increasing in VLSI circuits. Therefore reduce of power consumption in switching activity at the I/O ports can save significant save of power. Change of voltage level on the wires significant power consumptions. As the technology scaled down, the increased wire aspect ratio (height/width) reduce the spacing between individual bus wires. This resulted in the domination of coupling capacitance. There are so many techniques have been proposed to reduce the coupling activity along with the self-switching activity. Initially, Bus invert method can be applied to encode buses without prior knowledge of data statistics. Another encoding technique called "Sequence Switch Coding for low-power data transmission" (SSC) was proposed by Myungchul Yoon to minimize Self Transition activity in buses. Among the Bus Invert method and Sequence Switch Coding, the Bus Invert method has gained popularity because of its better energy reduction (upto25.45%). However, both Bus Inver and SSC bus encoding techniques reduce only self transitions and do not consider the effect of coupling transitions. Therefore, it is important to minimize the power dissipation and cross talk delay by minimizing the both self transitions and coupling transitions on bus for the fast and safe VLSI circuits. A new technique is introduced by doing some modifications to existing SSC technique given by Myungchul Yoon et.al, to reduce the energy dissipation and delay on DSM bus through encoding the data on the bus.

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### Introduction

As CMOS processes scale down to sub micron dimensions, power associated with system buses and the I/O accounts for a large portion of the total system power. Many encoding schemes have been presented to reduce the power dissipation on buses. In deep sub micron technologies, the coupling capacitances are becoming dominant for the total energy dissipation on buses. Various techniques have been proposed to reduce the power dissipation due to switching activity on bus. Thus, the power on bus can be reduced by reducing the transition activity on buses.

The Intrinsic capacitances of the bus lines, a sufficient amount of power is required at I/O lines of system when data travelled on the bus. Power has become an important design criterion in battery operated systems. There are many encoding schemes in the literature gives how to reduce the power consumption on buses. The main sources of power dissipation [1] in VLSI circuits are the leakage currents, the standby currents, short circuit currents. Power reduction techniques have been proposed at different levels of the design algorithmic and system level to layout level and circuit level.

The main power dissipation in the circuits due to the capacitive current and is given by  $P=1/2 CL V_{dd}^2 E(SW)f_{clk}$ . Where P is the power dissipation, CL is the physical capacitance at the output of the node, V<sub>dd</sub> is the supply voltage,  $f_{clk}$  is the clock frequency and E(SW) is the average number of output transitions per 1/ f<sub>clk</sub> time.

The main research work have focused on reducing the dynamic power consumed by reducing the number of change of states on the bus. Mainly focus in the reduce power consumption on off chip buses since power dissipated on the I/O pads of aC

ranges from 10% to 80% of total power consumed by the total circuit.

### Existing works on bus encoding

Since the instruction addresses are mostly sequential, Gray coding [3] was proposed to minimize the transitions on the instruction address bus. The Gray code ensures that when the data is sequential, there is only one transition between two consecutive data words. However this coding scheme may not work for data address buses because the data addresses are typically not sequential. An encoding scheme called T0 coding [4] was proposed for the instruction address bus. This coding uses an extra bit line, an increment bit-line along with the address bus, which is set when the addresses on the bus are sequential, in which case the data on the address bus is not altered. When the addresses are not sequential, the actual address is put on the address bus. Bus-Invert (BI) coding [2] is proposed for reducing the number of transitions on a bus. In this scheme, before the data is put on the bus, the number of transitions that might occur with respect to the previously transmitted data is computed. If the transition count is more than half the bus width, the data is inverted and put on the bus. An extra bit line is used to signal the inversion on the bus. Variants of T0, T0\_BI, Dual T0, and Dual T0\_BI [5] are proposed which combines T0 coding with Bus-Invert coding. Ramprasad et al. described a generic encoder-decoder architecture [6], which can be customized to obtain an entire class of coding schemes for reducing transitions. The same authors proposed INC-XOR coding, which reduces the transitions on the instruction address bus better than any other existing technique. An adaptive encoding method is also proposed by Ramprasad et al. [6], but

with huge hardware overhead. This scheme uses a RAM to keep track of the input data probabilities, which are used to code the data. Another adaptive encoding scheme is proposed by Benini et al., which does encoding based on the analysis of previous N data samples [7]. This again has huge computational overhead. Mussol et al. propose a Working Zone Encoding (WZE) technique [8], which works on the principle of locality. Although this technique gives good results for data address buses, there is a huge delay and hardware overhead involved in encoding and decoding. Moreover this technique requires more extra bit lines leading to redundancy in space.

There are so many techniques have been proposed to reduce the coupling activity along with the self-switching activity. Initially, Bus invert method [2] can be applied to encode buses without prior knowledge of data statistics.

Another encoding technique called "Sequence Switch Coding for low-power data transmission" (SSC) [9] was proposed by Myungchul Yoon. In this technique, the number of self transitions (ST) of two successive data items is measured at a time with respect to the previously transmitted data on bus. Among them, the data with minimum self transitions is selected for transmission (winner), while the other data item is held as a logger for the next computation of self transitions. Among the Bus Invert method and Sequence Switch Coding, the Bus Invert method has gained popularity because of its better energy reduction (upto25.45%). Both techniques need one extra wire (one wire redundancy) to send the coding information to the decoder. They reduce only self transitions and do not consider the effect of coupling transitions.

The sequence switch coding [9] method, proposed a technique to reduce self switching activity on the buses by rearranging of the data. It is suitable for both random data and stream type of data. It also needs one extra line to send the control information to indicate that the data is present data or the next data. In another method called Shift Invert coding for Low Power VLSI [10], for each data, its inverted value, shift left equivalent value, shift right equivalent value are considered. This technique did not concentrate on coupling activity.

The techniques of Bus invert [2], Sequential Switch Coding [9] and Shift Invert method [10] are incomplete in the sense that they minimize only the self transitions in reducing the total power dissipation. The technique "Odd/Even bus invert with two phase transfer for buses with coupling," (OE-BI) introduced by Yan Zhang et al., [11] finds relevance in this context. It considers reduction of both self and coupling transitions. However it requires more wire redundancy than Bus Invert and Sequential Switch Coding techniques.

The proposed techniques in this paper are modified version of the Sequential Switch Coding given by Myungchul Yoon [9] and the modified procedure is given below to which we have developed and obtained better reduction in energy and delay .

#### Characteristics of digital data:

Practically observed, in the execution of program 15% of the instructions are branches or jumps, means that on instruction address bus there will be a change of address sequence 15% of the time and remaining 85% of the time be sequential access. Since address on the instruction bus are sequential most of the time.

Let us assume L is the length of the sequential data and W is the size of the data (AW-1, AW-2, ... A1, A0)

The least significant bits change of level 100% of the time. The total number of change of states is a sequence of data L to be a  $\sim 2(i+1)$ , irrespective of the length of sequential data.

It follows that lines 0,1,2 contributes  $\sim 87.5\%$  of the total number of changes that occur on the sequential data.

The bit lines have recurring patterns with the recurring pattern length equal to  $2(i+1)$  for bit position i.

Like multimedia systems, many applications require a file or streaming data rather than a few bytes of granulated data as the input/output for their basic operations. The I/O data are transferred consecutively at a relatively constant rate. This kind of transfer pattern gives us a new opportunity to reduce the number of bus transitions during data transmission. When a sequence of data moves through a bus, its transmission sequence can be chosen to minimize the number of bus transitions [9]

#### Proposed coding technique

Steps for the proposed algorithm:

Read a file.

Measure the total no. of coupling transitions and self transitions of the given file.

Initialize the status of the 8-bit bus.

Initialize the control line S to '0'.

Read next 8 bit data.

Measure the coupling transitions Ct, of the data.

Measure and note the hamming distance between the data on the bus and the 8 bit data, St (self transitions).

Measure Total transitions,  $Tt1 = Ct + St$ .

Read the next data.

Measure the coupling transitions, Ct of the data.

Measure and note the hamming distance between the data on the bus and the 8 bit data, St (self transitions).

Total transitions,  $Tt2 = Ct + St$ .

If  $Tt1 < Tt2$ ,

Put new data on the bus, and make S=1 and transmit;

If  $Tt1 > Tt2$ , put previous data on the bus, and make S=0 and transmit;

Do steps 5 to 15 till the end of the file.

#### Simulation results

The above proposed technique is simulated using random function in C language software and tested with  $10^5$  random vectors. This technique is aimed to reduce energy dissipation and achieves 25% reduction in energy dissipation in DSM technology inter connects. It is observed that the energy due to the coupling transitions and delay play a major role when technology shrinks.

#### Conclusion and future work

A new transition reduction scheme is proposed in this paper. It considers both self and coupling transitions. Our future work is to test various ways to switch a data sequence, and to develop efficient ways for their implementation. The modifications done in our work to the Sequential Switch Coding given by Myungchul Yoon [9] performs well in reducing the power, and cross talk delay which are the two important sources need to be considered in low power VLSI design.

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