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Modified analysis of Rathore – Bhattacharya analog multiplier

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ABSTRACT

The four quadrant analog multiplier proposed by Rathor and Bhattacharya is reanalysed and modified in a different way for simple and low cost multiplication applications without using any reference waveforms. Verification of the feasibility of the circuit configuration is established by way of test results.

Introduction

If the width of a pulse train is made proportional to one voltage and the amplitude of the pulses to a second voltage, then the average value of pulse waveform is proportional to the product of two voltages, is called time division multiplier or sigma delta multiplier [1] – [3]. These multipliers require a source of highly linear, symmetrical triangular wave as reference. In the alternate way time division multiplier is developed using sawtooth wave as reference [4] – [6] . Rathore and Bhattacharya proposed a multiplier [7] using time division principle but without using any triangle or sawtooth waves as reference clock. This circuit [7] is redesigned, analysed with modifications and described in this letter.

Circuit Analysis

The circuit diagram of proposed analog multiplier is shown in Fig. 1 and its associated waveforms in Fig. 2. ±Vcc is the power supply to the circuit. The input voltage V_1 is given to the non-inverting terminal of the integrator OA_1. Let initially the comparator OA_2 output is –Vcc, integrator OA_1 output will be

$$V_S = \frac{1}{R_1C_1}\int (Vcc+V_1)dt - V_T = \frac{(Vcc+V_1)}{R_1C_1}t - V_T \quad (1)$$

The output of the integrator OA_1, V_S is linearly increasing and when it reaches a voltage V_T, the comparator OA_2 output changes from –Vcc to +Vcc and hence the integrator OA_1 output will be

$$V_S = -\frac{1}{R_1C_1}\int (Vcc-V_1)dt + V_T = -\left[\frac{(Vcc-V_1)}{R_1C_1}\right]t + V_T \quad (2)$$

The output of integrator OA_1 is linearly decreasing from V_T and when it reaches $-V_T$, the comparator OA_2 output becomes –Vcc and the cycle therefore repeats. The V_T is give as

$$\pm V_T = \pm Vcc\frac{R_3}{R_4} \quad (3)$$

From the waveforms shown in Fig. 2 it is observed that

$$T_1 = \frac{Vcc-V_1}{2Vcc}T \quad (4)$$

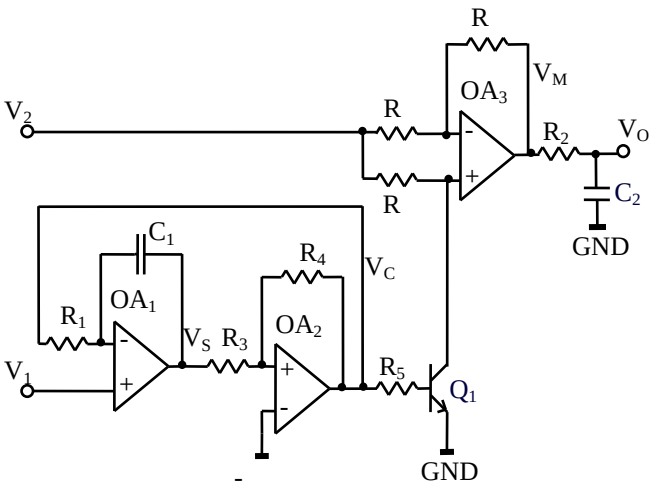

Fig. 1 Modified Rathore – Bhatacharya multiplier

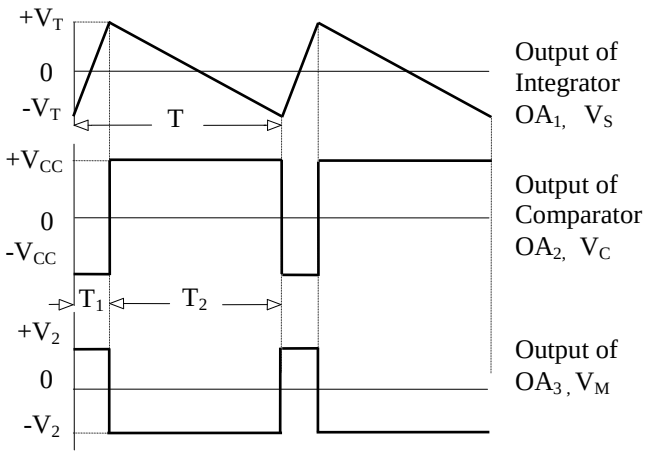

Fig. 2 Associated waveforms of Fig. 1

$$T_2 = \frac{Vcc+V_1}{2Vcc}T \quad (5)$$

$$T = T_1 + T_2 \quad (6)$$

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The comparator OA_2 output V_C controls the amplifier OA_3. The second input voltage V_2 is given to the control amplifier. During ON time of V_C, the transistor Q_1 is ON and shorts non inverting terminal of OA_3 to GND and hence OA_3 will work as inverting amplifier. The output of OA_3 V_M will be $-V_2$. During OFF time of V_C, the transistor Q_1 is OFF and hence OA_3 will work as non- inverting amplifier. The output of OA_3 V_M will be V_2. Hence a asymmetrical square wave V_M of inverted V_C and peak to peak of $\pm V_2$ is generated at the output of the control amplifier OA_3. The R_2C_2 low pass filter gives average value of this pulse train. Hence the output will be

$$V_O = \frac{1}{T}\left[\int_0^{T_2}(-V_2)dt + \int_{T_2}^{T_1+T_2} V_2 dt\right] \quad (7)$$

$$V_O = \frac{1}{T}\left[-V_2T_2 + V_2(T_1+T_2) - V_2T_2\right] \quad (8)$$

$$V_O = \frac{V_2}{T}(T_1 - T_2) \quad (9)$$

Equations (4) and (5) in (9) gives

$$V_O = -\frac{V_1V_2}{Vcc} \quad (10)$$

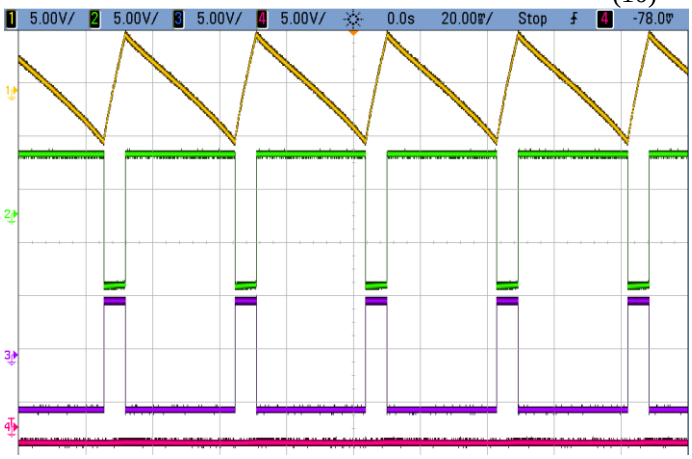

Fig. 3. Waveforms of Fig. 1 observed in a DSO. Top(1) to Bottom (4) details; (1) output of integrator OA_1, V_S (2) output of comparator OA_2, V_C (3) output of control amplifier OA_3, V_M (4) RC Low pass filter Output V_O.

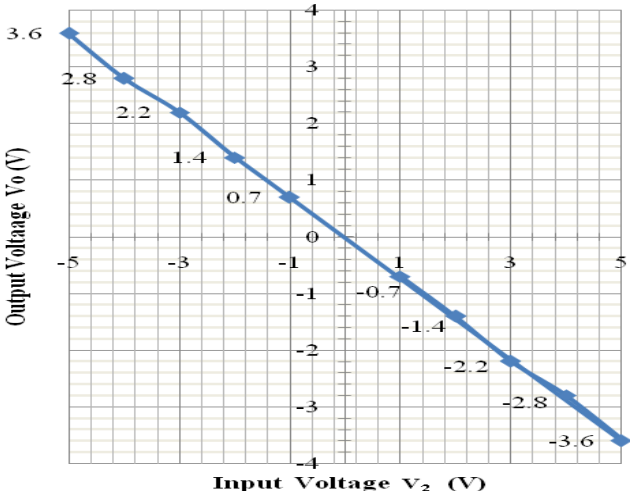

Fig. 4 Test results of Fig. 1 (V_1= 5.2V, Vcc = 6V)

Experimental Results And Conclusion

The proposed circuit is tested in our laboratory. LF 356 ICs are used for all op-amps OA_1-OA_3. A power supply of $\pm$Vcc = $\pm$7.5V is chosen. The observed waveforms are shown in Fig. 3. In practical the peak to peak value of comparator is found to be $\pm$6V. Hence in equation (10) the given Vcc is 6V. The test results for varying V_2 from -1V to -5V and 1V to 5V by keeping constant V_1 = 5.2V are shown in graph of Fig. 4.

A simple, low cost and accurate four quadrant analog multiplier is described. The accuracy is depending on the power supply voltage. Hence a precision power supply is to be used for the circuit. The other way is to connect two voltage references in series across the output of comparator OA_2 to limit its saturating levels which determines the multiplication constant. The proposed circuit can be used for active, reactive and apparent power measurements. They can also be used for phase sensitive detectors to find applications in impedance measurements.

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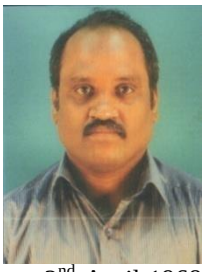

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