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Sub threshold source coupled logic based design of low power CMOS analog multiplexer

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ABSTRACT

A novel approach for designing Ultra Low Power and wide dynamic range circuit for multiplexing analog signals is presented. The design operates in weak inversion (Sub threshold) region and uses Source - Coupled Logic (SCL) circuit. The bias current of the SCL gates is varied to scale down linearly the power consumption and the operating frequency. The multiplexer design employs CMOS transistors as transmission gate with dynamic threshold voltage. The design exhibits low power dissipation, high dynamic range and good linearity. The design was implemented in 180 nm technology and was operated at a supply voltage of 400 mV with a bias current ranging in the order of few pA. The ON and OFF resistance of the transmission gate achieved were 27 ohms and 10 M ohms respectively. The power dissipation achieved is around 0.79 µW for a dynamic range of 1µV to 0.4 V.

Introduction

This work basically highlights on the applicability of sub-threshold source coupled logic (STSCL) for building analog circuits and systems that run at very low voltage and obligation to provide enticing performance with exquisite energy savings. Fields like bio-medical engineering need very less energy consumption for long battery life. Besides meeting the ultra-low power specification, the system must also be reliable and should function under harsh conditions. In this work, logic gates are designed and analyzed using STSCL. These gates are used for implementation of analog subsystems which would operate at very low supply voltages and consume very less power.

The switch finds many applications in integrated circuit design. In analog circuits, the switch is employed to implement useful areas like multiplexing, modulation and other applications. It is used as a transmission gate in digital circuits and adds a dimension of flexibility as found in standard logic circuits. The implementation of Ultra Low Power Systems has proved to the quite pivoted in many modern applications in many areas like mobile systems [1],[2] sensor networks[3],[4], and implantable biomedical applications [5]. Low power has gained more importance in today's electronics industry. The Necessity for low power has caused a major paradigm shift where power dissipation has become significant consideration in performance and area wise.

CMOS switches have great characteristics and in its most important form, a voltage-controlled resistor which offers very low resistance less than 100 Ω in its ON state and very High resistance of several hundreds of Mega ohms in OFF state with Pico-ampere leakage currents. CMOS technology is compatible with logic circuitry and integrates large number of ICs. [6]. Its fast switching characteristics are well controlled with minimum circuit leakage. MOSFET transistors can switch positive and negative voltages and conduct positive and negative currents with equal ease.

Implementation of high performance systems especially for low power applications creates many challenges and requires the trade off among speed of operation, power consumption, supply voltage and device parameters such as threshold voltage and oxide thickness in conventional CMOS technology.

When the MOSFET is in sub threshold operation the trans conductance to bias current ratio of the transistor is maximum and the current density is very low [7], [8]. On the other hand, for implementing widely adjustable circuits the exponential relationship between drain current and gate voltage makes this mode of operation well suited [7], [9]. The dynamic (switching) power consumption which is quadratically dependent on the supply voltage will cause the CMOS logic circuits utilizing sub threshold region transistors operate with a very low power consumption [10]–[13]. Therefore reduction in supply voltage reduces power dissipation and also output voltage swing [1], [14] thereby increasing the delay in each gate. This means the power dissipation, logic swing, and speed of operation are related to each other. The control of power consumption becomes difficult due to the exponential relation between power dissipation and supply voltage in sub threshold region. To implement very low power systems it is necessary to minimize the power dissipation at the system level in addition to the gate level for achieving desired performance [10].

This paper presents a new topology for implementing analog switch for ultra low power applications. For achieving this a novel approach for implementing Source Coupled Logic (SCL) circuits biased in sub threshold region is described. The speed of operation is independent of supply voltage and threshold voltage of devices. In addition the current consumption in each cell can be brought down to few pico-Amperes. It is therefore possible to reduce the system power consumption well below the sub threshold leakage current of conventional CMOS circuits. To enable operation at very low current levels and to attain the desired performance specifications, special circuit techniques have to be applied for implementing very low power SCL circuits.

The work focuses on the technique for implementing subthreshold (STSCL) gates where the bias current of each cell

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can be set as low as 10pA. A brief review of SCL circuits, the proposed technique for implementing the low power analog switch using sub threshold SCL gates, power consumption and experimental results are described in the following sections.

Subthreshold Source-Coupled Logic Circuits

The speed of operation in an SCL gate is inherently high as the logic operation mainly takes place in current domain. An nMOS source coupled differential pair transistors acts as a switch to steer the tail current Iss to one of the output depending on the input logic. The Load resistor R_L converts this current to output voltage to drive the other SCL gates. In order to switch the input differential pair of the next stage the output voltage swing (R_L I_{SS}) should be adequately high. Based on this the drain source over drive voltage input pair should be larger than $\sqrt{2}$ n V_{dssat} when Vin = 0.

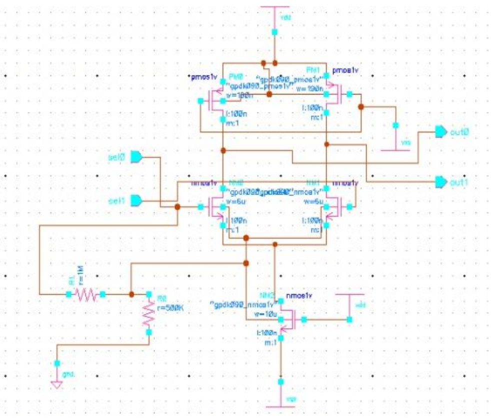

Fig. 1. Source Coupled Logic-based inverter/buffer circuit.

A source coupled logic based inverter/ buffer circuit is shown in FIG 1. More complex logic functions can be implemented by using a complex network of nMOS source coupled pairs as switching part [7,13]. The load resistance R_L is implemented by biasing the pMOS device in triode region and also nMOS switching network should be arranged in a proper way to achieve desired logic operation. The input logic level steers the tail bias current into one of the branch of the source coupled pair and this current is converted to voltage by the load resistance. The DC response of the SCL circuit is given in FIG 2.

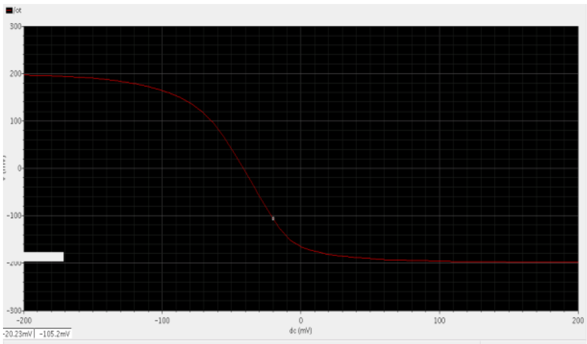

Fig 2. DC response of the SCL circuit

Operating in subthreshold regime, the device transconductance strongly depends on temperature through U, while it does not depend on device sizes. Therefore, it is not possible to change the transfer curve by design parameters [12]

Voltage Swing: One of the main advantages of SCL topology is the possibility of reducing the signal swing. Compared to the CMOS topology where the signal swing is equal to VDD, in SCL topology voltage swing and hence the current needed for charging and discharging the parasitic capacitances is less. Using as a logic circuit, the voltage swing at the input and output of the circuit should be high enough to make sure that the tail bias current will be completely switched to one of the two output branches. In other words, the voltage swing at the output node, i.e.:

$$V_{SW} = R_L \cdot I_{SS}$$

It should be high enough to switch completely the input differential pair of the next stage.

$$V_{SW} > V_{SW,min}$$

Which is equivalent to say that the gain of each SCL circuit should be high enough to be used as a logic circuit with acceptable noise margin. The minimum acceptable voltage swing at the output of each SCL gate, i.e., Vsw, $_{min}$, depends on the region of operation of NMOS devices [17,18]:

$$V_{SW,min} = \begin{cases} \sqrt{2} \cdot n \cdot V_{DS_{sat}} & \text{in strong inversion,} \\ 4 \cdot n \cdot U_T & \text{in subthreshold} \end{cases}$$

Where n is the subthreshold slope factor of NMOS devices. Biased in subthreshold regime, the minimum acceptable value for input swing can be reduced to 4.n.U_T, which is about 150mV at room temperature (assuming n = 1.5). SCL gate biased in subthreshold region utilizes a pMOS load device as shown in FIG 1. All devices operate in subthreshold region and the tail bias current can be reduced until it becomes comparable in magnitude to the leakage currents that exist in the circuit. Since the input differential pair transistors are operating in subthreshold, it can be shown that the transconductance of the input differential pair is

$$G_M = \frac{\partial I_{OUT}}{\partial V_{IN}} = \left(\frac{I_{SS}}{2n_n U_T}\right) \cdot \frac{1}{\cosh^2(V_{IN}/(2n_n U_T))}$$

pMOS and nMOS Transistors can be combined as shown in FIG 3 as transmission gate for implementing analog switch which selectively allows or blocks the signal from input to output. The transistors are turned ON or OFF by applying control signals to the gates in complimentary manner and at the output a drop in signal amplitude is observed. This problem is eliminated by modifying the transmission gate by stacking transistors and the signal is passed to the output without any loss.

Body Biasing

The voltage difference between the Transistors Source and the Bulk (V_{SB}) will effect the change in Transistor Threshold voltage V_T. Since V_{SB} effects V_T the bulk can be treated as second Gate that helps to identify how the transistor turns On and OFF.

Body effect refers to the change in the transistor threshold voltage (V_T) resulting from a voltage difference between the transistor source and body. Because the voltage difference between the source and body affects the V_T, the body can be thought of as a second gate that helps determine how the transistor turns ON and OFF. The strength of the body effect is usually quantified by the body coefficient γ(gamma). The threshold voltage of MOSFET is well known as,

$$V_{Th} = V_{Th0} + \gamma_B(\sqrt{|2\phi_F + V_{SB}|} - (\sqrt{|2\phi_F|})$$

where V_{SB} is the voltage between source and bulk, ϕ_F is the bulk Fermi- potential ,V_{Th0} is the threshold voltage when V_{SB}=0 and γ_B is the body-effect coefficient. Therefore varying threshold voltage Vth can be changed by varying V_{SB} which can form dynamic threshold voltage MOSFET (DTMOS). Normally, the source and body junction is either zero-biased or reverse-biased. Forward-body-biased MOSFETs can also be used on some circuit to improve performance with lower threshold voltage

VTh [10]. This concept is utilized in designing the power analog multiplexer. The transistors are operated in strong inversion region by means of using 0.4 V forward body bias.

Varieties of body biasing techniques are enabled by strong body effect and these techniques are effectively utilized in older generation. This body bias can be applied externally (external to the chip) or internally (in chip). The internal approach normally utilizes a charge pump circuit provide reverse body bias or potential divider to produce forward body bias. Reverse body bias for an n channel transistors increases the threshold voltage and makes the transistors both slow and less leakage. On the other hand forward body bias reduces the threshold voltage making the transistor fast and with more leakage. The polarities of the body bias are opposite for P channel transistor. The transmission gate with body bias is given in FIG 3.

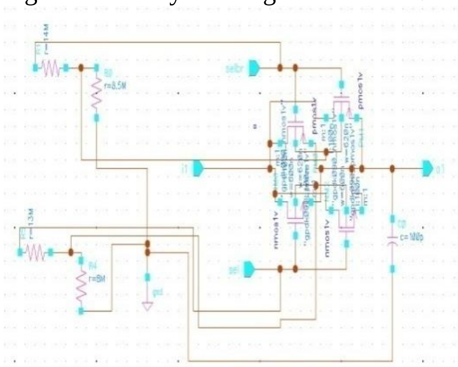

Fig 3. Transmission gate with dynamic body bias

Multiplexer Design

Using the concept of a shift register large number of multiplexers designed in the past. Synchronously triggered D-latches using external clock connected serially are used to build shift register. Each D-latch enables one S & H circuit. The clock feed-through to the output line is the major disadvantage of this circuit. With each clock cycle glitches occur synchronously for every positive and negative clock edge. The proposed multiplexer design minimizes this problem.

Instead of setting the body bias just once either during design or at production test, the Dynamic body bias changes the body bias many times when the chip is operating. The temperature and aging effects are minimized by Dynamic body bias and also the power management modes for optimizing very low power operation are effectively utilized [7], [8].

A logic '1' on SEL signal at the gate of nMOS transistors will turn them ON and a complimentary SELBR connected to the gate of pMOS transistors will turn them ON and the applied signal is allowed to pass from IN to OUT. On the other hand when the SEL is at logic'0' and its complimentary SELBR will turn all the transistots OFF thereby blocking the signal from IN to OUT. The output will be forced into a high-impedance state during the transition period from on to off where the junction capacitance will be charged to few millivolts.

A pMOS transistor connected as a pass transistor between the ground and the output node minimizes this problem. Whenever all the transistors are in off state then the pmos transistor will be turned ON, forcing the output capacitor to discharge to ground.

The widths of the transistors are maintained in a ratio of 1:2 for NMOS to PMOS. The on resistance R_{on} of the switch is

$$Ron = \frac{1}{g_{ds}} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{Th})}$$

The value of the ON-resistance depends on the overdrive voltage, $V_{ov} = V_{gs} - V_{th}$ and on the aspect ratio, W/L through the transconductance parameter µCox.

An analog loss less multiplexer with eight channels has been designed using this modified circuit shown in FIG-3 for each channel. The channels are selected by three binary control inputs. The inhibit input is used to Enable or Disable the multiplexer. A low ON resistance of 27 ohms, high OFF resistance of 10Mohms,with very low leakage current in the order of Pico amperes were obtained with the analog transmission gate.

STSCL Gates & Decoder Design

The logic gate designed using STSCL is AND gate and the schematic is given in the FIG 4 below. The circuit is simulated and analyzed so that nominal parameters of the STSCL can used which will produce an optimum level output for the system.

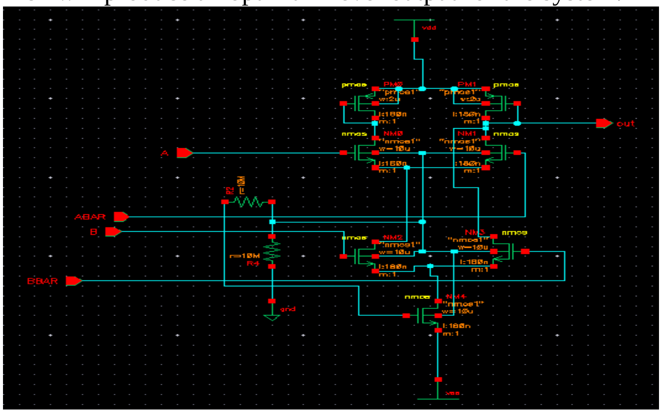

Fig 4: Source coupled logic AND gate

A 3to 8 decoder implemented using the above SCL AND gate. This is used to generate the select signals for each channel from three binary control inputs. The block diagram and the circuit diagram of the system is shown in FIG 5(a) & (b).

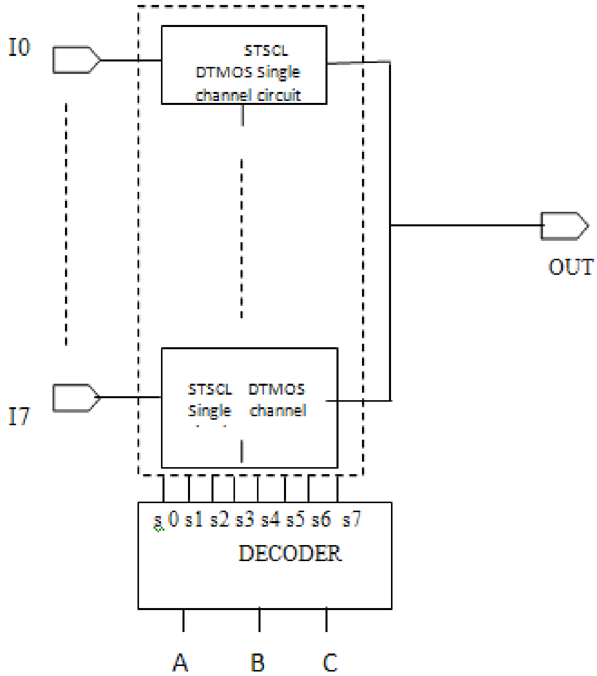

Fig: 5(a). Block diagram of 8:1 mux with decoder

Results:

The dynamic body bias is provided by means of potential divider using poly resistors for both nMOS and pMOS devices. A capacitor of 100pf is used to reduce the leakage at the output. The Inverter and Buffer output of the SCL gate drives the nMOS and pMOS devices. The circuit is verified with input signals with different amplitudes and frequency. When the SCL output signal is a Logic 0 pMOS transistors are turned ON and the complementary Logic 1 is applied to nMOS transistors to turn ON which allows the signal to pass from IN to OUT. When the signal goes to Logic 1, all transistors are turned off blocking the input signal. During the transition period from on to off the output will be forced into a high-impedance state where the junction capacitance will be charged to few millivolts.

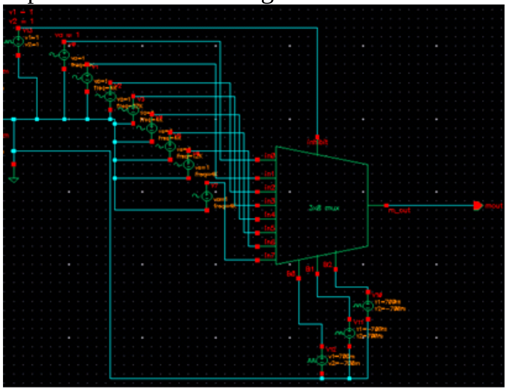

Fig 5(b) : circuit diagram of 8 channel MUX

To avoid this drawback, a pMOS transistor is used between the output node and ground as a pass transistor. When all the transistors are in off state, the pmos transistor turns ON forcing the output capacitor to discharge to ground. The system is simulated by applying sinusoidal input of 1µV amplitude and the frequency is varied from 1Hz onwards upto 1kHz.The total current drawn by the circuit is around 1.98 µA resulting in the total power consumption of 0.78µW. The response of the system is shown in FIG's 6(a),(b),(c). As the frequency of the input signal is increased the power dissipation increased.

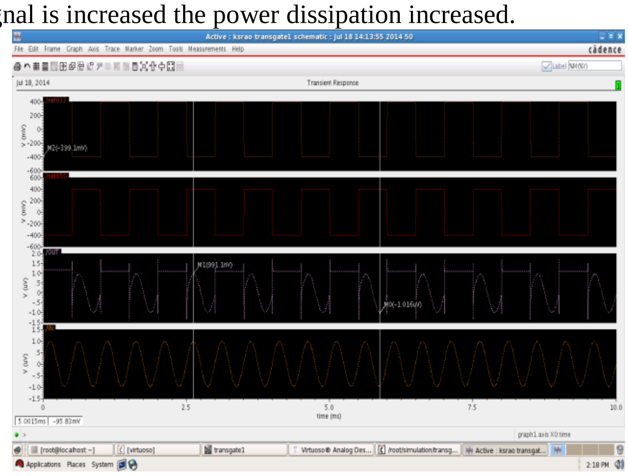

Fig 6(a): Simulated output with 1µV / 1KHz sinewave

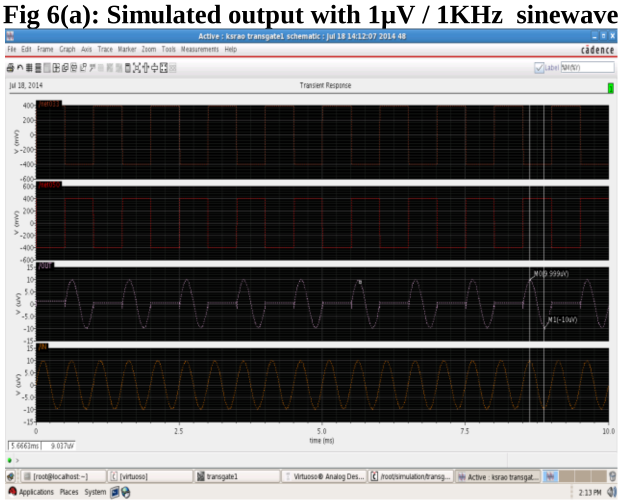

Fig 6(b): Simulated output with 10µV / 1KHz sinewave

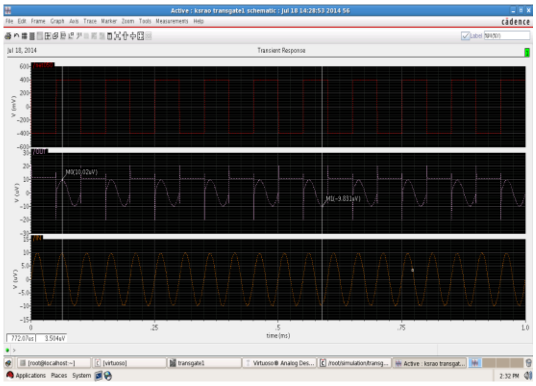

Fig 6(c): Simulated output with 10µV / 10KHz sinewave

The circuit is simulated by applying sinusoidal signals with an amplitude ranging from 1uV to maximum of 0.4V to each channel. The channels are selected by changing the input control signals of the decoder and the desired input is selected as shown in table-1

Table-1

Inhibit	Inputs	C	B	A	Output
L	X	X	X	X	L
H	I0	L	L	L	I0
H	I1	L	L	H	I1
H	I2	L	H	L	I2
H	I3	L	H	H	I3
H	I4	H	L	L	I4
H	I5	H	L	H	I5
H	I6	H	H	L	I6
H	I7	H	H	H	I7

The channel selection frequency is varied from DC to 10KHz. The output voltage is obtained without any distortion and the simulated results are shown in the Figures. 7(a), 7(b) and 7(c).

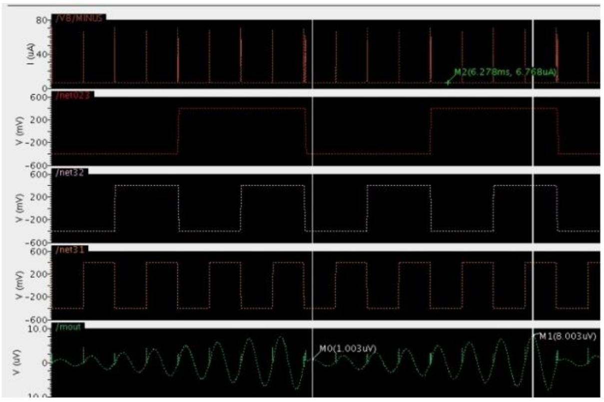

Fig: 7(a) simulated results with an amplitude of 1µV

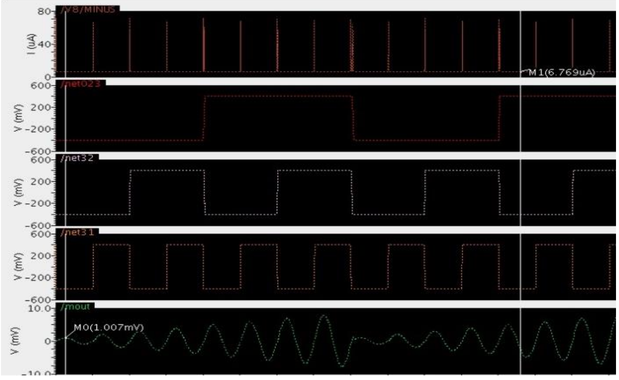

Fig: 7(b)simulated results with an amplitude of 1mV

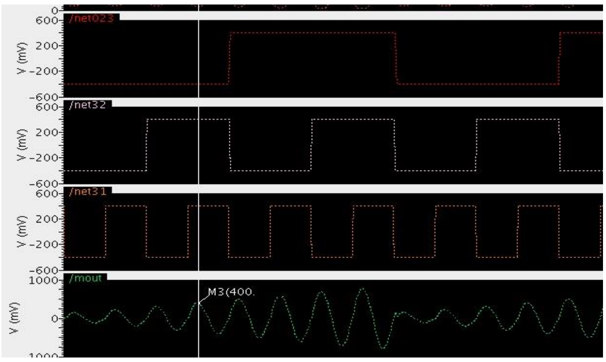

Fig: 7(c) simulated results with an amplitude of 100mV to 400mV

Conclusions:

A low power wide range source coupled logic circuits operated in subthreshold region for switching analog signals is implemented in 180nm technology using CADENCE TOOLS. The required output voltage swing for proper logic operation is provided by using high resistance pMOS load devices. Transmission gate circuit was used to switch analog signals with amplitude ranging from 1µV onwards. The On and OFF resistance of the gate achieved was 27 ohms and 10M ohms respectively. The total power dissipated at a switching frequency of 10KHz is around 0.79µW. The STSCL circuit was used to implement 8 channel multiplexer for acquiring biomedical signals and the power dissipated was measured as 0.79 µW. The number of channels to multiplexed can be increased further with suitable additional circuitry.

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