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Design and Analysis of Area and Power Efficient Tree Topology Based Multiplexer

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ABSTRACT

In this paper a power and area efficient design of 32:1 tree type multiplexer has been designed by hybridizing GDI and PTL techniques. Multiplexer circuit using this technique consumes less power in comparison to the CMOS, TG and other logic design techniques. The proposed design consists of 63 NMOS and 31 PMOS. At 1.2 V power supply the proposed MUX design consumes 47.093 µW power on BSIM-4 and 47.09 µW power on LEVEL-3 with simulation length of 5n. The proposed multiplexer is designed and simulated using DSCH 3.1 and MICROWIND 3.1 on 180nm.

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Introduction

Multiplexers are key components in CMOS memory elements and data manipulation structures. The various approaches have been proposed to reduce power consumption of MUX trees. The increasing requirement for low-power very large scale (VLSI) can assigned at different design levels, such as the architectural, circuit, layout, and the process technology level. Multiplexer abbreviated as MUX is the heart of any arithmetic circuit. MUX are a common building block for data paths and data-switching structures, and are used effectively in a number of applications including processors, processor buses, network switches, and DSPs with resource sharing [1]. Multiplexer is basically a digital switch. The multiplexer has numbers of input data lines and one output line. The selection of a particular input line is controlled by a set of selection lines. This paper utilizes the concept of GDI PTL technique in the design of multiplexer using 180 nm technology. A tree-type multiplexer is composed of multiple 2-to-1 MUX cells organized in a tree structure.

Gate diffusion input

Gate diffusion input method is used for designing low power and fast circuits with less number of transistors. The GDI method is based on the use of a simple cell as shown in Figure 1:

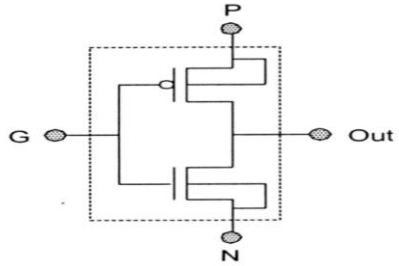

Figure 1. GDI basic cell [2]

Table 1 shows the different functions performed by basic GDI cell:

Table 1. Various Logic functions performed by GDI cell for different input combinations:

N	P	G	OUT	FUNCTION
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT

Pass Transistor Logic

The pass transistor logic is used to reduce the count of transistors required for logic implementation than the same function implemented with the same transistors in complementary CMOS logic. The advantage is that single pass-transistor network (either PMOS or NMOS) is enough to perform the logic operation.

32:1 GDI PTL MUX

In this section 32:1 MUX circuit has been designed by using GDI PTL technique. This schematic consists of 63 NMOS and 31 PMOS with total of 94 transistors and the power consumed by the circuit is 47.093 µW at BSIM-4 with input voltage supply of 1.2 V. The logic diagram of proposed 32:1 GDI PTL MUX is shown as shown in figure 2:

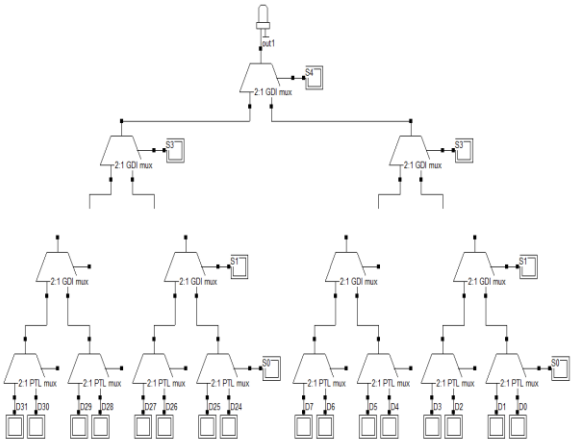

Figure 2. 2:1 MUX based proposed 32:1 MUX tree

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In this design, Gate Diffusion input with Pass transistor logic kind of MUX structure is enforced with terribly minimum transistors compared to the CMOS and transmission gate based design. So, in the proposed design power consumption is reduced with minimum space. Figure-3 shows the schematic of 32:1 MUX which consists of 31 2:1 MUXS in a tree type structure as:-

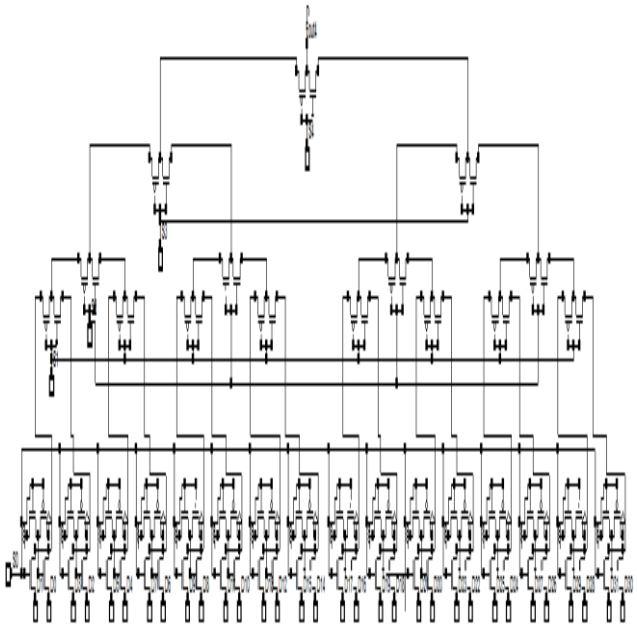

Figure 3. 32:1 GDI PTL MUX

The layout simulation of 32:1 MUX is shown in figure 4 as:

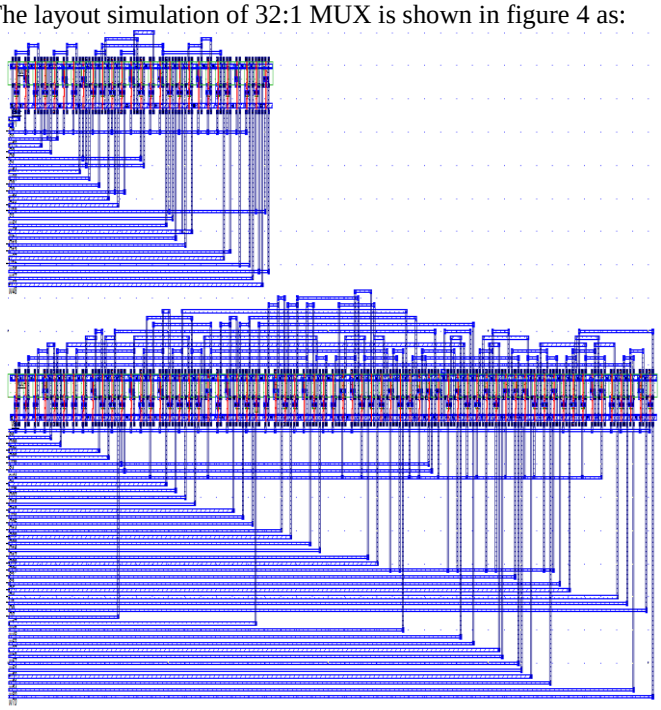

Figure 4. Layout of 32:1 GDI PTL MUX

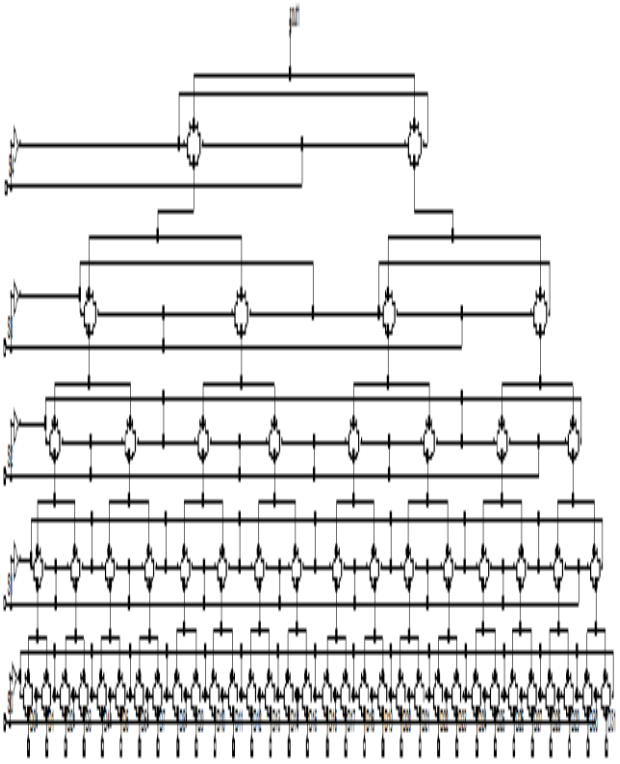

Figure 5a. 32:1 TG MUX

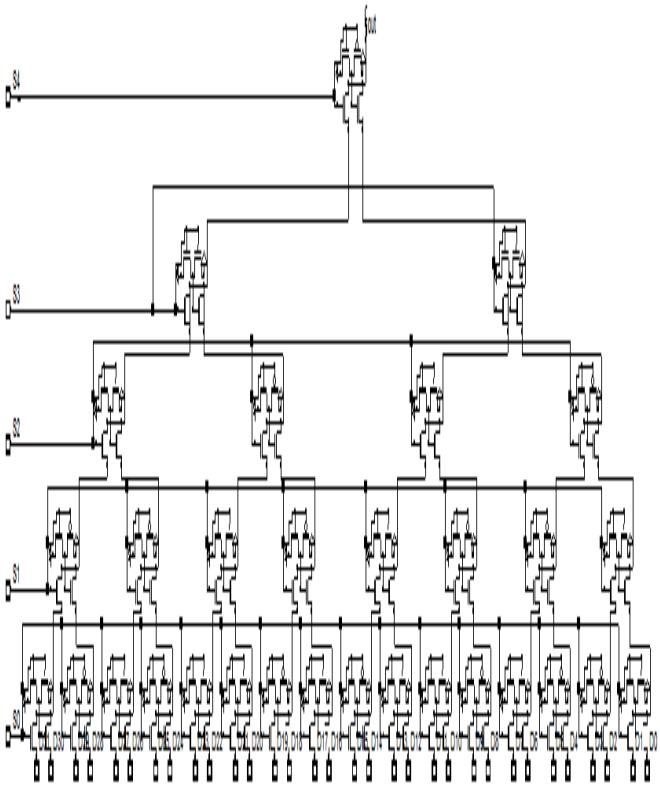

Figure 5b. 32:1 PTL MUX

Figure 5. 32:1 MUX Designs using different logic

Figure 5 shows the 32:1 MUX circuits composed of 31-2:1 MUX circuits in a tree type structure by using transmission gate and pass transistor logic designs. The number of NMOS and PMOS required for transmission gate 32:1 MUX are 67 and 67 respectively with a total transistor count of 134 and for pass transistor logic design there are 93 NMOS and 31 PMOS used and in this case transistor count is 104. Different logic designs are compared in terms of transistor count which reflects the total area and also in terms of total power consumed. In table 1 we

can see that the area and power consumed by the proposed 32:1 MUX is minimum which is 47.093 µW in comparison with the power consumed by Pass transistor, CMOS, Transmission gate, AND and NAND based MUX designs. Comparative analysis of different 32:1 MUX designs by different logics on 180 nm technology has been shown in the table 2 as:-

Table 2. Comparison of proposed 32:1 MUX in terms of area and power with other 32:1 MUX designs by different logics on 180nm technology

32:1 MUX design	NMOS	PMOS	Area (µm^2)	Power (µW)
GDI PTL	63	31	20401.7	47.093
PTL	93	37	23849.3	350
CMOS	178	178	42516.5	596
TG	67	67	22226.9	97.399
AND	284	283	29903.3	256
NAND	191	191	19169.3	206

Simulation Results

The performance of proposed 32:1 MUX design has been evaluated in terms of area and power on 180nm technology. Simulation has been performed using MICROWIND 3.1. Time simulation for proposed 32:1 MUX has been done on 180 nm as:-

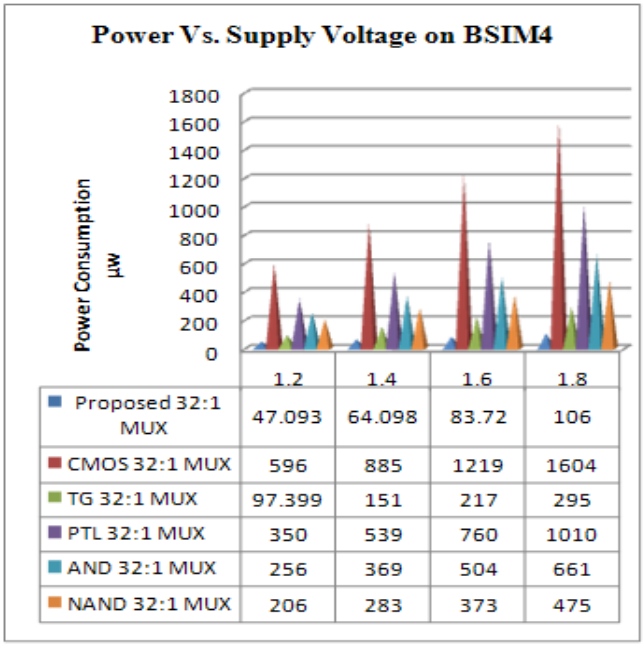

Figure 6. Comparison of Power Consumption on BSIM4

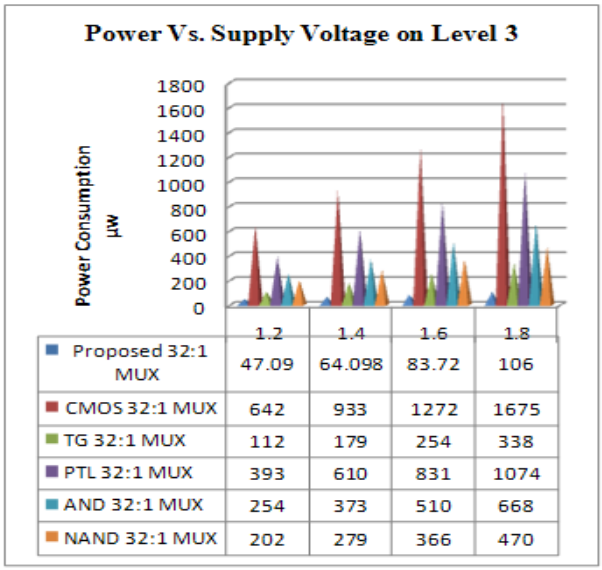

Figure 7. Comparison of Power Consumption on Level 3

From figure 6 and 7 it is clear that the power consumption decreases with decrease in input supply voltage. Results are measured in terms of variation in power with respect to the variation in voltage on BSIM-4 and LEVEL-3. The analog simulation has been obtained to know the power consumption at different voltage by using MICROWIND 3.1. Analog simulation is carried out for proposed 32:1 MUX on 180nm technology. For 180nm VDD is fixed to 1.2 V and VSS to 0V.

Conclusion

Proposed 32:1 MUX has been realized in 180-nm CMOS technology which consists only 94 transistors. Proposed 32:1 PTL MUX design has been implemented by using 63 NMOS and 31 PMOS transistors. Area and simulation of proposed 32:1 MUX design has been shown on 180nm with simulation length of 5n. The simulation results have been shown on LEVEL-3 and BSIM-4 models. Proposed 32:1 MUX using 94 transistors consumes power 47.093 µW at BSIM-4 model and consumes power 47.09 µW at LEVEL-3. Results show that power consumed by the proposed GDI PTL 32:1 multiplexer has shown reduction in power consumption by 92%, 86%, 52%, 82% and 77% as compared to CMOS, PTL, TG, AND and NAND logic techniques respectively on BSIM-4 simulation model is on 180nm technology. All the results are simulated using MICROWIND3.1.

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