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A New Form of Quarter – Squarer Multiplier

K.C.Selvam

Department of Electrical Engineering, Indian Institute of Technology Madras, Chennai – 600 036, India.

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ABSTRACT

An implementation of quarter – squarer multiplication using op-amps is described. It uses op-amp based dual squaring circuits. It eliminates the drawback of MOSFETs based quarter squarer multiplier. Verification of the feasibility of circuit configuration is established by way of test results on a proto type.

Introduction

A multiplier is one which accepts two voltages and produces an output voltage proportional to the product of two input voltages. There are several methods for analog multiplication. logarithmic function generator, FET multiplier, triangle averaging multiplier, magneto resistance multiplier and transconductance multiplier are few examples. Four types of analog multiplier are reported in [1]. They are (1) Time division multiplier (2) Pulse width integrated multiplier (3) Double single slope multiplier and (4) Pulse position sampled multiplier. The first commercial analog multiplier is Quarter – Squarer multiplier using MOSFETs[2]. This technique is based on the algebraic identity

$$xy = \frac{1}{4}[(x+y)^2 - (x-y)^2] \quad (1)$$

Summing amplifiers and squaring circuits are involved in this technique. This was based on the piecewise – linear approximation technique which uses diode breakpoint networks. The most drawback of this multiplier is that it has relatively large errors for small inputs, even though the maximum error is a small percentage of full scale. The input voltage is converted in to a pulse width δ_T and a reference voltage is integrated during the time width δ_T. The average value of the integrated output is proportional to square of the input voltage [3]. The quarter squarer multiplier using this principle with op-amps is described in this paper.

Circuit Analysis

The proposed circuit diagram is shown in Fig. 1 and its associated waveforms in Fig. 2. A sawtooth wave of peak V_R is generated by the opemaps OA_1, OA_2 and switch S_1 [4]. OA_1 is a integrator that forces the feedback capacitor C_1 to charge at a rate set by the input current I whose value is V_R/ R_1. For proper operation, this current must always flow out of OA_1's summing junction; hence V_R can take only negative values. During capacitor charge, the comparator OA_2 output is at the LOW state and switch S_1 is in OFF state. The output of the integrator OA_1 is given as

$$V_S = \frac{1}{R_1C_1}\int V_R dt = \frac{V_R}{R_1C_1}t \quad (1)$$

When the output of the integrator OA_1 exceeds the reference voltage V_R, the comparator OA_2 output is HIGH and the switch S_1 shorts the capacitor C_1, Hence V_S comes down to 0V. The comparator OA_2 is prevented from responding immediately to this change because of the charge accumulated in C_1 during the comparator's output transition from 0V to +Vcc. After timing out, the comparator OA_2 output returns to LOW and the switch is opened allowing C_1 to resume charging. The cycle, therefore, repeats itself at a period T. The waveforms thus generated are shown in Fig. 2. From the waveforms shown in Fig. 2 and from the equation (1) by the fact that at t = T, V_S = V_R.

$$V_R = \frac{V_R}{R_1C_1}T$$
$$T = R_1C_1 \quad (2)$$

The inputs V_1 and V_2 are given to adder OA_3 and subs tractor OA_4. Their outputs are given as

$$V_X = V_1 + V_2$$
$$V_Y = V_1 - V_2 \quad (3)$$

The output voltage of OA_3, V_X is given to the comparator OA_5 which compares this with the sawtooth waveform. A rectangular asymmetric pulse waveform V_P is generated at the output of the comparator OA_5. Its OFF time δ_{T1} will be

$$\delta_{T1} = \frac{V_X}{V_R}T \quad (4)$$

The integrator OA_6 integrates the reference voltage $-V_R$ during the OFF time δ_{T1} by the switch S_2 (S_2 opens during OFF time and closes during ON time of δ_{T1}). A semi sawtooth wave $V_J(t)$ with peak value of V_J is generated at the output of OA_6. Its output will be

$$V_J(t) = \frac{1}{R_2C_2}\int V_R dt = \frac{V_R}{R_2C_2}t \quad (5)$$

From the waveforms shown in Fig. 2, at $t = \delta_{T1}$, $V_J(t) = V_J$

$$V_J = \frac{V_R}{R_2C_2}\delta_{T1} = V_X\frac{R_1C_1}{R_2C_2} \quad (6)$$

Tele:

E-mail addresses: kcselvam@ee.iitm.ac.in

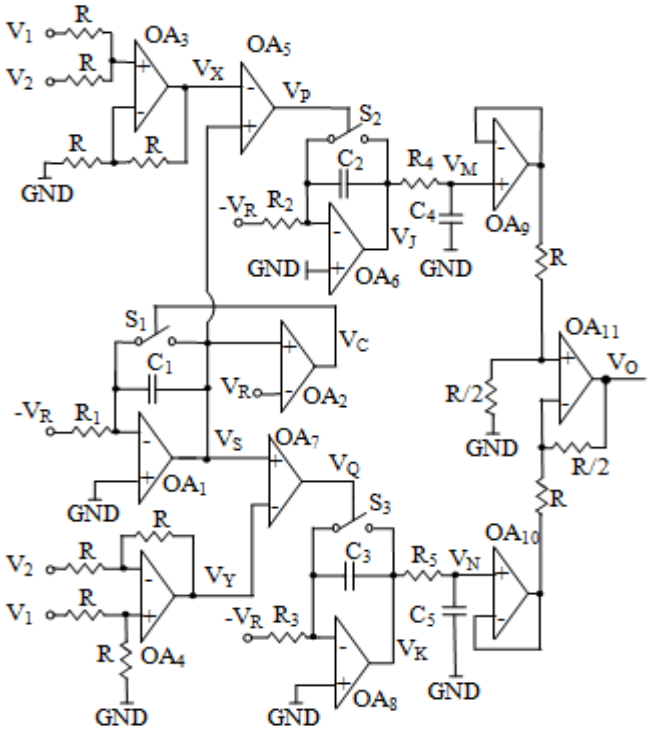

Fig 1. Circuit diagram of proposed quarter – squarer multiplier

Another voltage V_Y is also compared with the sawtooth wave by the comparator OA_7. A rectangular wave V_Q is generated at the output of comparator OA_7. Its OFF time δ_{T2} will be

$$\delta_{T2} = \frac{V_Y}{V_R} T \tag{7}$$

This pulse V_Q controls switch S_3 so that a similar semi-sawtooth wave $V_K(t)$ with peak value of V_K is generated at the integrator output OA_8. It will be

$$V_K(t) = \frac{1}{R_3C_3}\int V_R dt = \frac{V_R}{R_3C_3} t \tag{8}$$

From the waveforms shown in Fig, 2, at $t = \delta_{T2}$, $V_K(t) = V_K$

$$V_K = \frac{V_R}{R_3C_3}\delta_{T2}$$

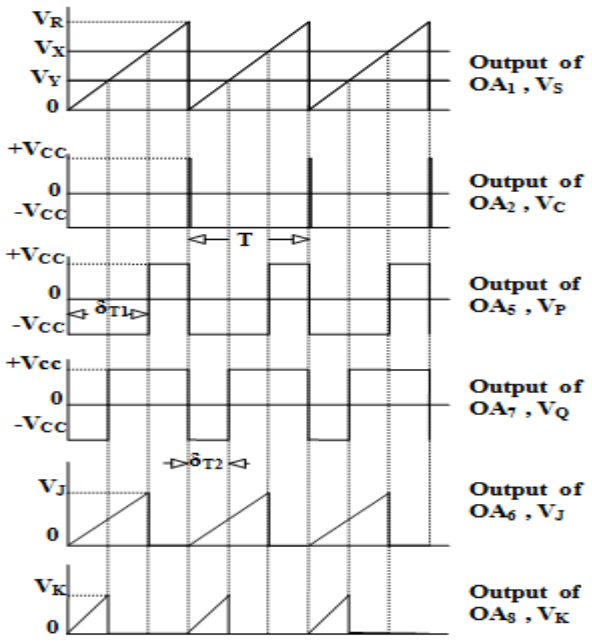

Fig 2. Associated waveforms of Fig. 1

$$V_K = V_Y \frac{R_1C_1}{R_3C_3} \tag{9}$$

The first semi-sawtooth $V_J(t)$ with peak value of V_J is given to the R_4C_4 low pass filter. Its output V_M will be

$$V_M = \frac{1}{T}\int_0^{\delta_{T1}} \frac{V_J}{\delta_{T1}} dt = \frac{V_J}{2T}\delta_{T1} \tag{10}$$

$$V_M = \frac{V_X V_J}{2V_R} = \frac{V_X^2}{2V_R}\frac{R_1C_1}{R_2C_2} = \frac{V_X^2}{2V_R} \tag{11}$$

(for $R_1 = R_2$, $C_1 = C_2$). Similarly the another semi - sawtooth $V_K(t)$ with peak value of V_K is given to the R_5C_5 low pass filter. Its output V_N will be

$$V_N = \frac{1}{T}\int_0^{\delta_{T2}} \frac{V_K}{\delta_{T2}} dt = \frac{V_K}{2T}\delta_{T2} \tag{12}$$

$$V_N = \frac{V_K V_Y}{2V_R} = \frac{V_Y^2}{2V_R}\frac{R_1C_1}{R_3C_3} = \frac{V_Y^2}{2V_R} \tag{13}$$

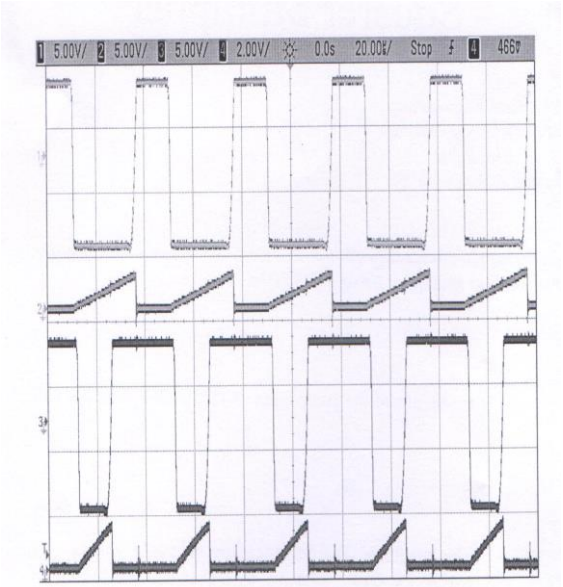

Fig 3. Practical Waveforms of Fig. 1 observed in a DSO. Top (1) to Bottom (4) details; (1) output of OA_5 V_P, (2) output of OA_6 V_J(3) Output of OA_7 V_Q and (4) output of OA_8 V_K.

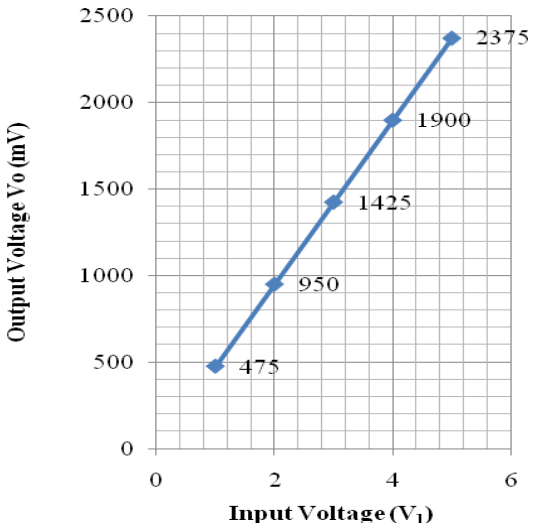

Fig 4. Test results (V_R=5V, V_2=2.5V)

(for $R_1 = R_3$, $C_1 = C_3$).The voltages V_M and V_N are given to the difference amplifier OA_{11}. The output of OA_{11} will be

$$V_O = \frac{1}{2}(V_M - V_N) = \frac{1}{4V_R}[V_X{}^2 - V_Y{}^2] \quad (14)$$

$$V_O = \frac{1}{4V_R}[(V_1 + V_2)^2 - (V_1 - V_2)^2] \quad (15)$$

$$V_O = \frac{V_1 V_2}{V_R} \quad (16)$$

Experimental Results And Conclusion

The circuit shown in Fig.1 is tested in our laboratory. The practical waveforms observed are shown in Fig. 3. A saw tooth wave of 5V peak (V_R) is generated for the experiment. LF 356 ICs are used for all op-amps OA_1-OA_9. CD4016 IC is used for all switches S_1-S_3.R_1=R_2=R_3=1M and $C_1 = C_2 = C_3$ =39pF are chosen. The test results are given in the graph of Fig. 4.

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References

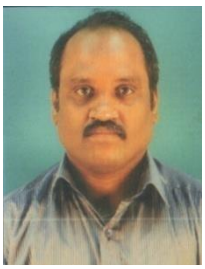
[1] K.C.Selvam, "Some Techniques of Analog Multiplication using Op-Amp based Sigma Generator", IETE Journal of Education, Vol.55, Issue 01, pp: 33-39 Jan – June 2014

[2] Y.J Wong and W.E.Ott, "Function Circuits; Design and Applications" Mc Graw-Hill Book Company, pp: 87-90, 1976

[3] C.Selvam and V.Jagadeesh Kumar, "A simple multiplier and squarer circuit", IETE Students Journal, Vol.37. Nos 1&2, Jan-Mar 1996, pp 7-10

[4] K.C.Selvam, "A Pulse Position Sampled Multiplier", IETE Journal of Education, Vol.54, Issue 1, pp: 5-8, Jan-Jun 2013.

Author photography and biography



K.C. Selvam was born on 2nd April 1968 in Krishnagiri District of Tamil Nadu State, India. He was graduated by the Institution of Electronics and Telecommunication Engineers, New Delhi, in the year 1994. He has published more than 25 research papers in various national and international journals. He got best paper award by IETE in the year 1996. At present he is working as Technical Staff in the Department of Electrical Engineering, Indian Institute of Technology, Madras, India. He developed interest in design and development of function circuits to find their applications in modern measurements and instrumentation systems.