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Characterization and Performance Investigation of Nanoscale MOSFETs

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ABSTRACT

A novel RF-MOSFET (Radio Frequency Metal Oxide Semiconductor Field Effect Transistor) model with PTM (Predictive technology model) for 90 nm CMOS (Complementary Metal Oxide Semiconductor) technology is presented. A simple and accuracy method is developed to directly extract all the high frequency parasitic effect from measured S-parameter biased at zero and linear region. This model is proposed to overcome some of short channel effects at nano-scale highly dopped drain and source based on the conventional small signal MOSFET (Metal Oxide Semiconductor Field Effect Transistor) equivalent circuit, RF (Radio Frequency) characterization of CMOS (Complementary Metal Oxide Semiconductor) has been taken up in terms of RF Figure of Merits. The excellent correspondence is achieved between simulated and measured S-parameter (Scattering parameter) from 1GHz to 10 GHz frequency range.

Introduction

For CMOS RFIC (Radio Frequency Integrated Circuit) development, developing circuits at high frequency and low voltage becomes a challenge, especially since most of the MOSFET models are not designed for either low voltage or high frequencies. Undesired interaction with a low resistivity substrate adds to the task of designing RF circuit on CMOS processes [1],. Device characterization and modeling at RF frequencies is necessary to allow accurate prediction of circuit performance prior to fabrication. The ultimate goal in modeling is a versatile model with few parameters (less than 20 parameters) and good performance in all the region of operation including high frequency of operation. [2].

MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths (x_{dD}, x_{dS}) of the source and drain junction. As the channel length L is reduced to increase both the operation speed and the number of components per chip, the so-called short-channel effects arise. [3]

In order to overcome the drawback of previously reported approaches, a novel model is presented to accurately predict the high frequency behavior of RF-MOSFET [4], [5]. A typical advanced MOSFET is shown in Figure 1. The complete new equivalent circuit small signal RF-model is shown in Figure 2.

RF characterization of CMOS has been taken up based on their respective small signal model. By doing Y- or Z- parameter analysis of their respective model and analytical procedure for parameter extraction has been developed and presented here. [4], [5].

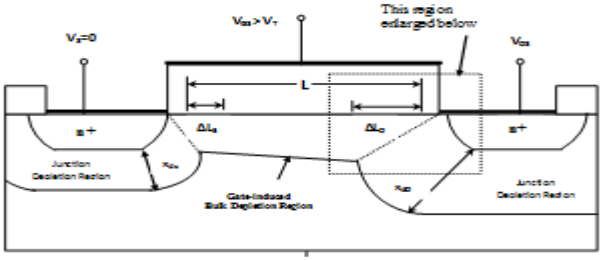

Figure 1. Cross-section of a typical advanced MOSFET

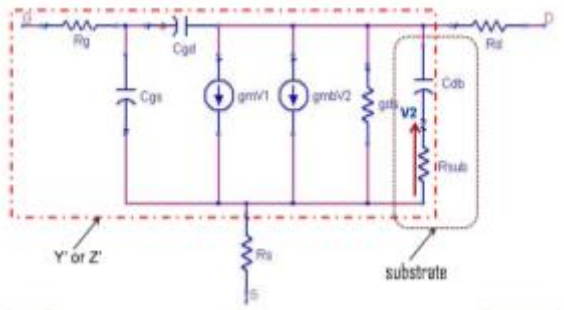

Figure 2. Small signal RF Model

The small signal RF model of Figure.2 has been used for analysis and the Y & Z parameters have been found in terms of the circuit parameters. The parameters are Gate resistance (R_g), drain resistance (R_d), source resistance (R_s), gate-to-drain capacitance (C_{gd}), drain-to-base capacitance (C_{db}), gate-to-source capacitance (C_{gs}), drain-to-source transconductance (g_{ds}), and the substrate parameters i.e. substrate resistance (R_{sub}), substrate capacitance (C_{db}).[1],[6],

Technology Specification

Table-1 [7]

Nano- CMOS: Technology node: 90 nm NMOS						
L_{eff}	T_{ox}	V_{dd}	V_{th}	R_{dsw}	I_{on}	I_{off}
35 nm	1.4 nm	1.2 V	0.2 V	180 Ω/μm	1100 (μA/μm)	50 (nA/μm)

RF Model Development

To have an efficient design environment, design tools with accurate models for devices and interconnect parasitics are essential. It has been known that for analog and RF applications the accuracy of circuit simulations can be strongly determined by the device models. Accurate device models become crucial to correctly predict the circuit performance. [8]

For a model to describe the device characteristics accurately, all important model parameters should be extracted from the actually Fabricated NMOS device [10]. The RF model development steps are shown using a flowchart shown in figure 3.

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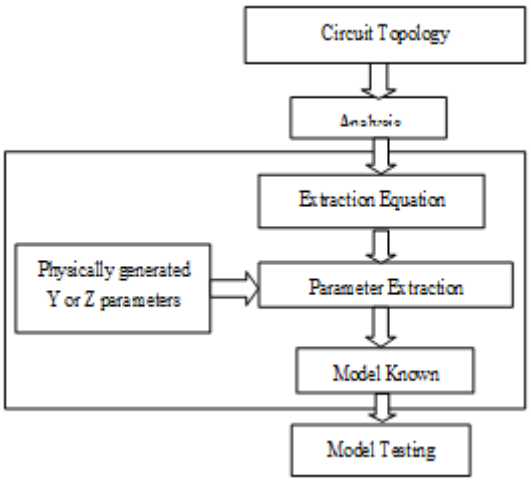

Figure 3. Flowchart for Model

Fabrication of Nanoscale MOSFET

Here fabrication of nanoscale MOSFET is performed using ATLAS (SILVACO) TCAD tool. LDD (Lightly Doped Drain) is used to overcome device degradation short channel effects [8], and improved a lot but still have a chance of improvement. Heavily doped drain and source, lightly doped drain and source extensions and lightest doping of gate are done. The device structure of fabricated NMOSFET is shown in figure 4.

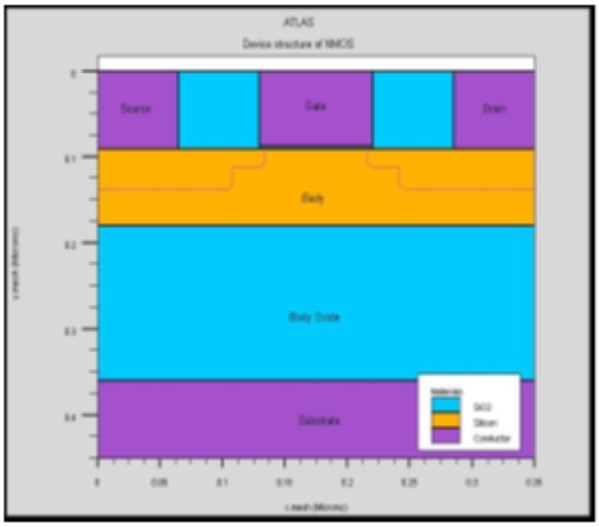

Figure 4 Device Structure of Fabricated-simulated MOSFET

Analysis and Parameter Extraction

The equivalent small signal RF model is shown in figure 2. Circuit analysis of the small signal RF model yielded the following results.

In the frequency ranges $\omega << [R_g(C_{gs}+C_{gd})]^{-1}$ and $\omega << [L_g(C_{gs}+C_{gd})]^{-1}$, a simplified expression for small signal Y-parameters $Y_{11}^{'}$, $Y_{21}^{'}$, $Y_{12}^{'}$, and $Y_{22}^{'}$ of the circuit enclosed by dashed line in Fig. 2 can be derived as: [2]

A. Y-parameters

$$Y_{11}^{'} \cong \omega^2 R_g (C_{gs}+C_{gd})^2 + j\omega(C_{gs}+C_{gd}) \quad \ldots(1)$$

$$Y_{21}^{'} \cong g_m - j\omega C_{gd} \quad \ldots..(2)$$

$$Y_{12}^{'} \cong -j\omega C_{gd} \quad (3)$$

$$Y_{22}^{'} \cong g_{ds} + j\omega C_{gd} + \frac{j\omega g_m R_{sub} C_{db}}{1+j\omega R_{sub}(C_{sub}+C_{db})} + \frac{j\omega C_{db}(1+j\omega R_{sub} C_{sub})}{1+j\omega R_{sub}(C_{sub}+C_{db})} \quad (4)$$

B. Z-parameters

$$\mathrm{Re}[Z_{12}] \cong R_s + BC_{gd}/(\omega^2 A^2 + B^2) \quad (5)$$

$$\mathrm{Im}[Z_{12}] \cong -\omega A C_{gd}/(\omega^2 A^2 + B^2) \quad (6)$$

$$\mathrm{Re}[Z_{22}] \cong R_s + R_d + (C_{gs}+C_{gd})B/(\omega^2 A^2 + B^2) \quad (7)$$

$$\mathrm{Im}[Z_{22}] \cong \omega B R_g (C_{gs}+C_{gd})^2 - \omega A (C_{gs}+C_{gd})^2/(\omega^2 A^2 + B^2) \quad (8)$$

Where,

$$A = C_{gd}C_{gs} + C_{db}(C_{gs}+C_{gd}) \quad (9)$$

$$B = g_{ds}(C_{gd}+C_{gs}) + g_m C_{gd} \quad (10)$$

In order to determine the other parameters, they can be shown in terms of real and imaginary part of $Y^{'}$ or $Z^{'}$ as shown below.

a) Transconductance,

$$g_m = \mathrm{Re}\,al(Y_{21}^{'}) \quad (11)$$

b) Drain-to-source transconductance,

$$g_{ds} = \mathrm{Re}\,al(Y_{22}^{'});\ \text{when } \omega \longrightarrow 0 \quad (12)$$

c) Gate resistance,

$$R_g = \mathrm{Re}\,al(Y_{11}^{'})/\mathrm{Im}(Y_{11}^{'})^2 \quad (13)$$

d) Gate-to-drain capacitance, $C_{gd} = -[\mathrm{Im}(Y_{12}^{'})]/\omega$ (14)

e) Gate-to-source capacitance $C_{gs} = [\mathrm{Im}(Y_{11}^{'})/\omega] - C_{gd}$ (15)

f) Extraction of Substrate Parameters R_{sub}, C_{db} *and* g_{mb}

The extraction equations are given as follows:

$$R_{sub} = \frac{\mathrm{Re}(Y_{22}) - g_{ds}}{(\mathrm{Im}(Y_{22}) + \mathrm{Im}(Y_{12}))^2 - g_{mb}(\mathrm{Re}(Y_{22}) - g_{ds}} \quad (16)$$

$$C_{db} = \frac{\mathrm{Re}(Y_{22}) - g_{ds}}{R_{sub}\omega(\mathrm{Im}(Y_{22}) + \mathrm{Im}(Y_{12})}\ , \quad (17)$$

$$g_{mb} \approx 0.2 \times g_m \quad (18)$$

Extraction Results

Table 2

For Vgs = 0.3 V Vds = 0 V , Rs = 3 Ω Rd = 5.95 Ω		
	Bias point 1 V_g = 0.3 V, V_d = 1.0 V	Bias point 2 V_g = 0.3 V, V_d = 1.5 V
g_m	3.8 mS	4.5 mS
g_{ds}	1.06 mS	1.241 mS
R_g	1.606 Ω	1.38 Ω
C_{gs}	319.07 fF	308.5 fF
C_{gd}	117.01 fF	112.96 fF
R_{sub}	22 mΩ	14.49 mΩ
C_{db}	90.0 fF	88.12 fF
g_{mb}	0.76 mS	0.9 mS

Short channel effects are studied and hence lightly doped drain and lightly doped source regions are considered to overcome these effects. ATLAS (Silvaco) TCAD tool is used for fabrication of MOSFET of channel length 90nm, gate oxide thickness as 2nm and threshold voltage 0.26V.

Model Testing

The component in the RF model has been determined, hence the RF model is known. For model testing, S-parameters of the model are generated and compared with the Fabricated NMOS Device S-parameters.

The comparison of Fabricated NMOS Device and modeled S-parameters will show that if the Fabricated NMOS Device and modeled plots are close then model is accurate within the permissible limit.

Comparison of Generated And Modelled S-Parameters

The comparison of the Modeled and Generated from Fabricated NMOS S-parameters is shown herewith. Fig.5 shows the comparison S-parameters at bias point 1 i.e. V_g = 0.3 V and V_d = 1.0 V.

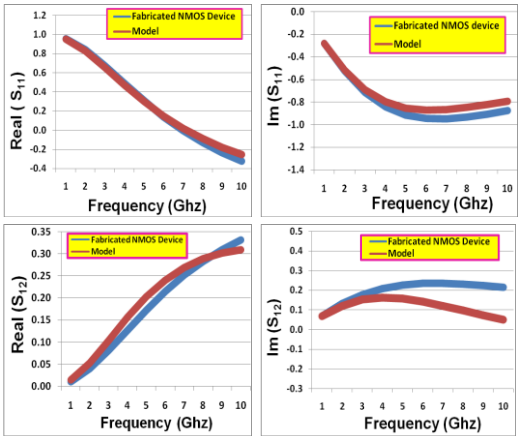

Figure. 5(a) Plot for S_{11} and S_{12} Vs Frequency at bias point 1

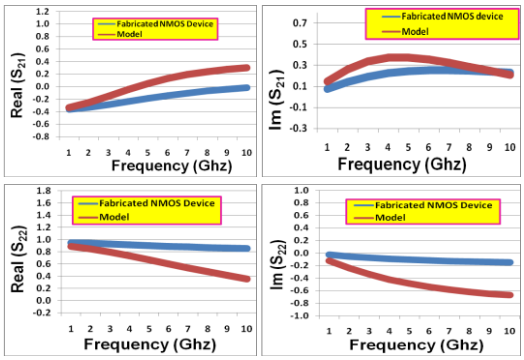

Figure. 5 (b) Plot for S_{21} and S_{22} Vs Frequency at bias point 1

RF Figure-of-Merits (FOMs)

f_T, f_{max} and Noise for CMOS

In the specific case of high frequency performance, two figure of merit are particularly popular. These are f_T and f_{max}, which are the frequency at which the current gain and power gain, respectively becomes unity. In the case of CMOS, for the expression of f_T ,[9] we assume that the drain is terminated at short circuit and the gate is driven by an ideal current source as shown in figure 6. The current source drive implies that the series gate resistance simply has no influence on f_T. The gate to drain capacitance is considered only in the computation of input impedance; its feed forward contribution to output current to gate current is given by-

$$\left|\frac{i_d}{i_{in}}\right| \approx \frac{g_m}{\omega(C_{gs}+C_{gd})} \tag{19}$$

$\left|\frac{i_d}{i_{in}}\right|$ has a value of unity at a frequency at a frequency given by

$$\omega_T = \frac{g_m}{(C_{gs}+C_{gd})} \tag{20}$$

therefore, $$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{21}$$

Computing f_{max} is a general quite difficult , so we will invoke several simplifying assumption to make an approximate derivation possible. We compute the input impedance with an incrementally shorted drain and ignore the feed forward current through C_{gd}. We do consider the feedback from drain to gate through C_{gd} in computing the output impedance, because computing of the maximum power gain requires termination in a conjugate match.

With the above assumptions, we can calculate the power delivered to the input by the current source drive as given by

$$P_{in} = \frac{i_{in} R_g}{2} \tag{22}$$

The magnitude of the short-circuit current gain at high frequencies from the Fig. 6, we can write

$$\left|\frac{i_d}{i_{in}}\right| \approx \frac{\omega_T}{\omega} \tag{23}$$

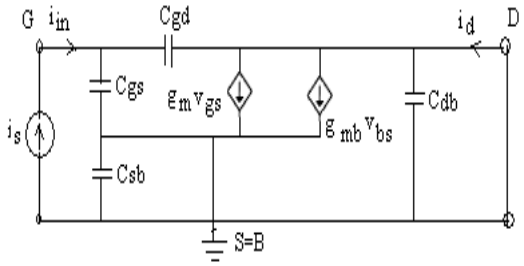

Figure. 6 MOSFET model including back gate effect (resistive element is not shown) shorted at drain and an ideal current source at the gate.

The resistive part of the output impedance is given by

$$g_{out} \approx g_m \cdot \frac{C_{gd}}{C_{gd}+C_{gs}} = \omega_T \cdot C_{gd} \tag{24}$$

If the conjugate termination has a conductance of the value given by (24), then the power gain will be maximized. The total maximum power gain is therefore given by

$$\frac{P_L}{P_{in}} \approx \frac{\frac{1}{2}\left(\frac{\omega_T}{\omega}\cdot i_{in}\cdot\frac{1}{2}\right)\frac{1}{(\omega_T \cdot C_{gd})}}{\frac{{i_{in}}^2 R_g}{2}} \approx \frac{\omega_T}{\omega^2 4 R_g C_{gd}} \tag{25}$$

From equation (25), $\frac{P_L}{P_{in}}$ has the value unity at frequency given by

$$\omega_{\max} \approx \frac{1}{2}\sqrt{\frac{\omega_T}{R_g C_{gd}}} \qquad (26)$$

Therefore, $$f_{\max} \approx \sqrt{\frac{f_T}{8\pi R_g C_{gd}}} \qquad (27)$$

The $f_{\max}$ is proportional to the square root of f_T and can be higher than f_T by minimizing the gate resistance.

Noise: Noise is generated in electronic circuits. That is, an electronic circuit will have output even without any input signal. Noise can be classified as one of five types:

Thermal noise, Shot noise, Flicker noise, Burst noise, and Avalanche noise

At RF thermal noise is important. A useful measure of the noise performance of a system is noise factor, usually denoted by F. The noise factor F and noise figure (NF) are defined as:

$$F = \frac{\text{Total output noise power}}{\text{Total output noise power due to the source}}$$

$$= \frac{\left(S/N\right)_{IN}}{\left(S/N\right)_{OUT}} \qquad (28)$$

$$\text{Noise Figure } (NF) = 10 * \log_{10}(F) \qquad (29)$$

Simulation: CMOS

Using Figure. 2, h_{21} is simulated at V_{GS} = 0.3 V and V_{DS} =1.0 V, and compared with measured data and result is shown in figure 8. Extending the plot along frequency axis we can find the approximate value of f_T at which current gain becomes 1. The approximate value of f_T can be obtained to be 40 GHz.

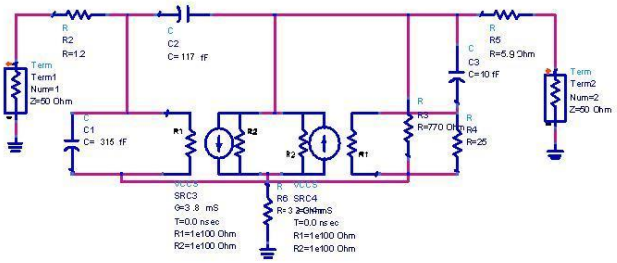

Figure: 7 ADS Simulation of equivalent circuit for CMOS

Simulated noise figure and result is shown in Fig. 8 and 9.

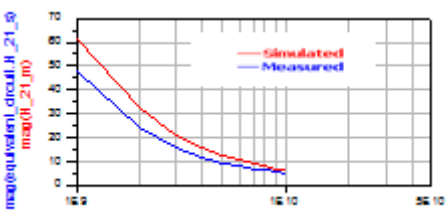

Figure: 8 Comparison of simulated and measured current gain for CMOS

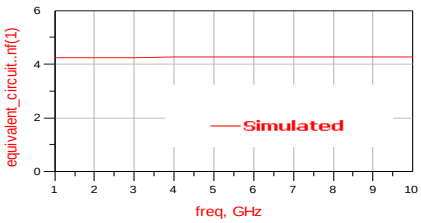

Figure: 9 Simulation result of noise figure for CMOS

Summary

The MOSFET has been successfully fabricated using ATLAS (SILVACO) TCAD tool. The device is solved for dc-vi characteristics and S-parameters are obtained. The component in the RF model has been determined, hence the RF model is known. For model testing, S-parameters of the model are generated and compared with the Fabricated NMOS Device S-parameters. To overcome some of the short channel effects at nano-scale lightly doped drain and source have been used. The coupling through the substrate is an important effect for mixed mode high-frequency IC design and should be appropriately accounted. At low frequency (<1GHz), it is good enough to model the substrate by a purely resistive network. However, at high frequency (>1GHz) where most of the wireless communication systems operate, both resistive and dielectric losses are important and must be appropriately modeled by a combination of R_{sub} and C_{db}. When this is done and appropriate account is taken of the back gate transconductance effect, a much more accurate RF model is developed, which can be used for evaluation output reflection coefficient in individual transistors as well as carrying out circuit design.

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