Available online at www.elixirpublishers.com (Elixir International Journal)

Advanced Engineering Informatics

Elixir Adv. Engg. Info. 90 (2016) 37940-37942

ISSN: 2229-712X

Simulation of 3 State Inverter Using Different Materials

Apurva Choubey and Rajesh Nema
NRI-Institute of Information Science & Technology, E.C.E Dept., Bhopal (M.P.), India.

ARTICLE INFO

Article history:
Received: 27 March 2013;
Received in revised form:
20 January 2016;
Accepted: 26 January 2016;

Keywords
Mosfet circuit,
Gallium arsenide,
Silicon nitride,
Silicon,
Silicon dioxide,
Power consumption.

ABSTRACT

This paper provides the simulation of 3 state inverter with different materials and compare the Leakage Current. Material which has the less Leakage Current is considered as better material for the designing of inverter. In previous time the mosfet is design by the combination of silicon and silicon oxide now we are using gallium arsenide and silicon dioxide as one combination and gallium arsenide and silicon nitride as another combination.

© 2016 Elixir All rights reserved.

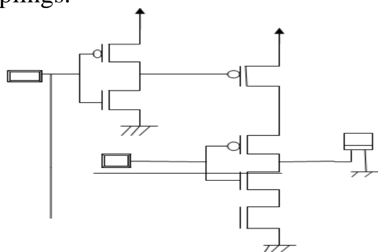
Introduction

The CMOS inverter design is consist of one p-channel MOS and one n-channel MOS transistors are used as switches. All the symbols produced the value logic '0' and logic '1'. However, if several inverters share the same node, such as bus structure conflicts will rise. In order to avoid multiple access at the same time, specific circuits called 3-state inverters are used, featuring the possibility to remain in a 'high impedance' state when access is not required.The 3-state inverter symbol consists of the logic inverter and an enable control circuit. The output remains in 'high impedance' (Logic symbol 'X') as long as the enable *En* is set to level '0'.

The truth table is reported below.

In	En	Out
0	0	X
0	1	1
1	0	X
1	1	0
X	0 or 1	X
0 or 1	X	X

The basic CMOS inverter is no more connected to the supply lines VDD and VSS directly. In contrary, pass nMOS and pMOS devices are inserted to disconnect the inverter when the cell is disabled. we see that when *Enable*=1 the cell acts as a regular CMOS inverter, while when *Enable*=0 the output "floats" in an unpredictable voltage value, which tends to fluctuate at the switching of the input, mainly due to parasitic leakage and couplings.



Properties of Materials

Gallium Arsenide

1.It has direct band gap, which means that it can be used to emit light efficiently.

2.Higher carrier mobilities and lower resistive device parasitic.

3.GaAs is an excellent material for space electronics and optical windows in high power application.

Silicon nitride

1.Silicon nitride is an important material in microelectronics due to its high resistivity, higher dielectric constant compared to silicon dioxide, mechanical strength and chemical inertness.

2.It is used as a gate insulator in thin flim transistor that are in flat panel display.

Silicon

1silicon is the existence of a native oxide (silicon dioxide), which is used as an insulator in electronics devices.

2. It has much higher hole mobility. This high mobility allows the fabrication of higher speed p-channel field effect transistor, which are required fo

Simulation

Gaas and al_2o_3

dielectric constant	oxide	semiconductor1	semiconductor2	current 1	current 2
K=3.9	SiO_2	GaAs	Ge	0.415 mA	0.049 mA
K=7.5	Si_3N_4	GaAs	Ge	0.428 mA	0.049 mA
K=9	Al_2O_3	GaAs	Ge	0.431 mA	0.049 mA
K=22	Ta_2O_5	GaAs	Ge	0.419mA	0.049 mA
K=25	HfO_2	GaAs	Ge	0.418 mA	0.049 mA
K=30	$LaAlO_3$	GaAs	Ge	0.418 mA	0.049 mA

Result

Output result :-

Gallium arsenide = 0.415

Germanium = 0.049

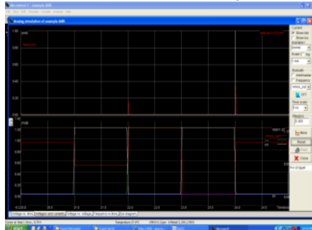
Tele:
E-mail addresses: apurva23choubey@gmail.com

© 2016 Elixir All rights reserved

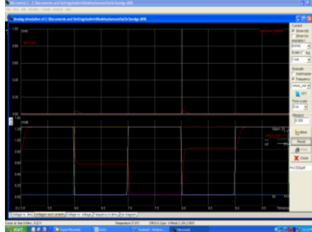
Error = 0.366
output in percentage = =88 %

Simulation

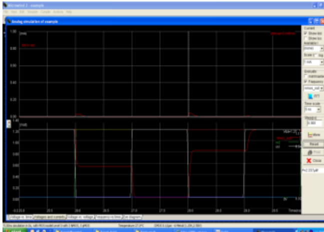
Gaas and al_2o_3



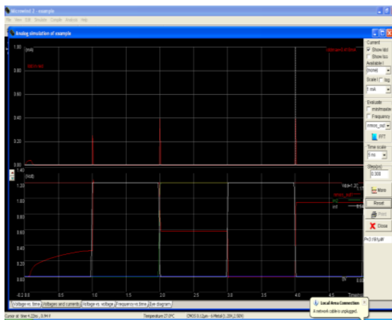
Ge and Al_2O_3



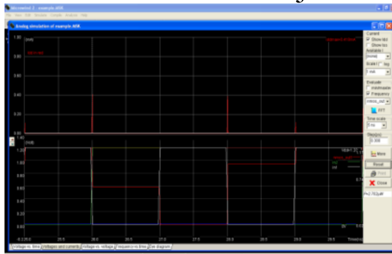
Ge and HfO_2



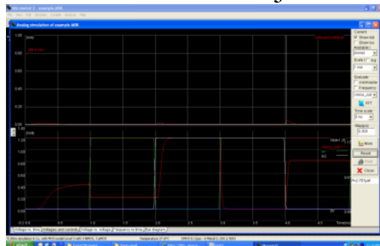
Ge and HfO_2



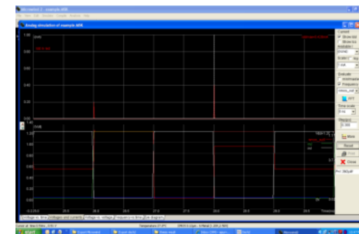
GaAs and $LaAlO_3$



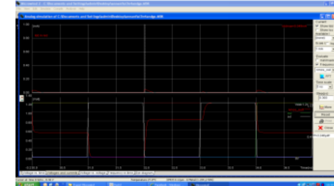
Ge and $LaAlO_3$



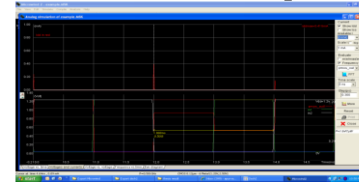
GaAs and Si_3N_4



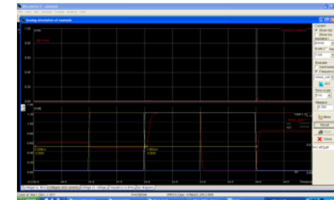
Ge and Si_3N_4



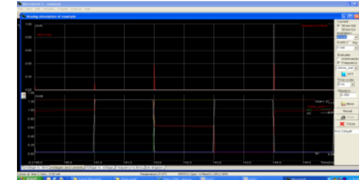
3.9GaAs and SiO_2



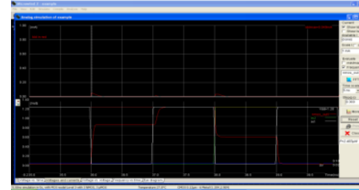
3.10Ge and SiO_2



3.11GaAs and Ta_2O_5



3.12Ge and Ta_2O_5



Conclusion

CMOS technology has seen an excellent high speed performance achieved through improved design, use of high quality materials and processing innovations over the past decade. Silicon dioxide gate dielectric is replaced with various high-k dielectric materials. The choice of the high-k dielectric and the knowledge of its physical properties helps in changing the various characteristics of the oxide layer
in respect to power, current and the layout area covered. It is observed that the leakage of the device decreases by about 88% . The study of the properties of these material was used in modeling the tri-state inverter and its various parameters were tabulated. The modeled inverter with high-k dielectric as gate dielectric material can be used for high gain and for low power applications in various electronic fields

References

[1] D Nirmal,P Vijay Kumar, "Nanoscale Tri Gate MOSFET for Ultra Low power applications Using High-K Dielectrics" Nanoelectronics Conference (INEC), 2013 IEEE 5th International.

[2]. D Nirmal,P Vijay Kumar," Nanoscale Channel Engineered Double Gate MOSFET for Mixed Region "International Journal of Circuit Theory and Application, 10 Mar 2012
[3]. J.Conde,A. Cerdeira et al," 3D Simulation of Triple Gate MOSFET with Different Mobility Region" Microelectronics engineering Vol 88, Issue 7,pp.1633-163,July 2011
[4] Kumar, M.P Gupta ,S.K Paul, "Corner effects in SOI tri gate FinFET structure by using 3D process and device simulation "Computer Science and Information Technology (ICCSIT), 2010