

1.8V 2.4/5.4 GHz CMOS Frequency Synthesizer with 32/33 Divider for 2.3/3.5 MHz Resolution

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ABSTRACT

The need for mobile communications computing and networking has turn out to be important more than ever. With the increasing demand for low cost and high integration of wireless transceiver building blocks, the low power is a great concern for Radio Frequency Integrated Circuit (RFIC) designers. Exhaustive exertion has been made to advance RF integrated circuits and systems in the GHz range using CMOS process in low cost. Frequency Synthesizer that includes Phase-Locked Loop (PLL) is a significant block of the transceiver this generates carrier for the down-conversion/up-conversion operations. Voltage-Controlled Oscillator (VCO) and High Frequency Divider (HFD) decides the channel selection of frequency synthesizer and power consumption. This work presents the design of 2.4/5.4 GHz CMOS Frequency Synthesizer for 2.3/3.5 MHz resolution with 32/33 divider circuit. The Frequency Synthesizer circuits are designed in 180nm CMOS process technology using Virtuoso of Cadence tools.

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1. Introduction

Shrinking feature size has really attracted the research and development of low-power Radio Frequency (RF) CMOS integrated circuits in last two decades. Low-power operations are of crucial significance for mobile wireless communications, as the battery lifetime is limited. The low power dissipation also helps to reduce the operating temperature resulting in more stable performance. A frequency synthesizer with low power VCO with quadrature signal generation and frequency dividers of low power with multi-channel selection is essential in the modern architecture of transceiver. Phase Locked Loops (PLL) are extensively used in radio frequency synthesis. One of the key building blocks of an RF front-end transceiver is the PLL based frequency synthesizer. The present wireless standards like Bluetooth and 802.11a/b/g offer comparatively high data rates at the expense of high power consumption and cost. The IEEE 802.15.4 standard has been precisely designed to cater for the needs of low cost, low power, low data rate and short range wireless networks. Generally the power consumption of a frequency synthesizer is reduced considerably by simplifying the circuit structures, and by adapting some low power techniques to the digital blocks such as frequency dividers. PLLs in frequency synthesizer, the concept of phase noise and its effect on the transceiver are facts to be considered.

II . Frequency Synthesizer

Phase Frequency Detector (PFD), Charge Pump (CP), Voltage-Controlled Oscillator (VCO), divider and Loop Filter (LF) are the building blocks of the frequency synthesizer. Frequency synthesizer generates a set of usually sinusoidal signals of given frequencies with the stability and precision referred to a single frequency reference source. It is regarded as one of the most critical modules in modern wireless communications systems. Figure 1 shows the architecture of a typical modern transceiver.

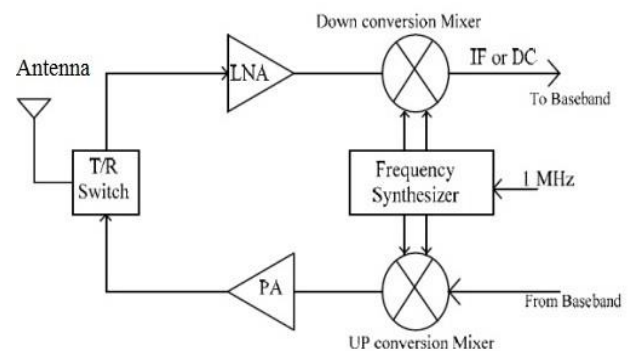


Fig 1. Frequency Synthesizers in the Transceivers.

Local Oscillator (LO) signal is used as the reference frequency signal for frequency translation and channel selection in communication systems. Therefore the output signal generated by the frequency synthesizer is normally called as local oscillator signal. At the receiver end, the high frequency LO signal is used to down-convert the incoming signal into a lower frequency baseband or Intermediate Frequency (IF). This signal can be processed to extract the information that is carried in the same LO signal which can be used to up-convert the baseband signal of an RF frequency to transmit over the medium. The frequency synthesizer is mainly designed to ensure the accuracy of its output signal under the operating given conditions. The frequency synthesizer is normally implemented using Phase Locked Loop (PLL)[1].

III. Design Methodology Of Frequency Synthesizer

A. Ultra-Low Power Prescaler

The high speed dual modulus prescaler uses wide-band pulse swallow frequency dividers and is a critical functional block in frequency synthesizer. This makes the prescaler to operate at the highest frequencies and consumes more power than other circuit blocks of the frequency synthesizer. The prescaler has two selectable division ratios N and $N+1$ in pulse swallow frequency divider [2].

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It is combined with programmable counters P and S as shown in Figure 2, to perform a programmable division ratio of $(N * P + S)$.

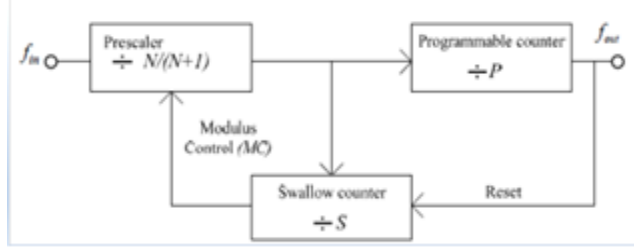


Fig 2 .Topology of the Pulse swallow frequency Divider.

B. Synchronous 2/3 Prescaler

An $N/(N+1)$ Dual Modulus Prescaler (DMP) consists of a synchronous prescaler followed by a series of asynchronous divide-by-2 circuits and additional logic gates to control the switching between the two different division ratios. Fig 3 shows the development of a simple 2/3 synchronous prescaler using divide-by-2 and divide-by-3 circuits. When control logic signal 'MC' is high, the output of OR gate is always equal to logic '1' and the output of AND gate is always equal to the inverted output of DFF2 (Q2) such that the prescaler operates in the divide-by-2 mode[3] as shown in Figure 3 (a). When control logic signal 'MC' is low, the output of OR gate is always equal to 'Q1', such that prescaler operates in the divide-by-3 mode as shown in Fig 3 (b). The output of the synchronous 2/3 prescaler shown in figure 3(c) is given by the following equation.

$$f_{out} = \overline{MC} * f_{in}/3 + f_{in}/2 \dots\dots\dots(1)$$

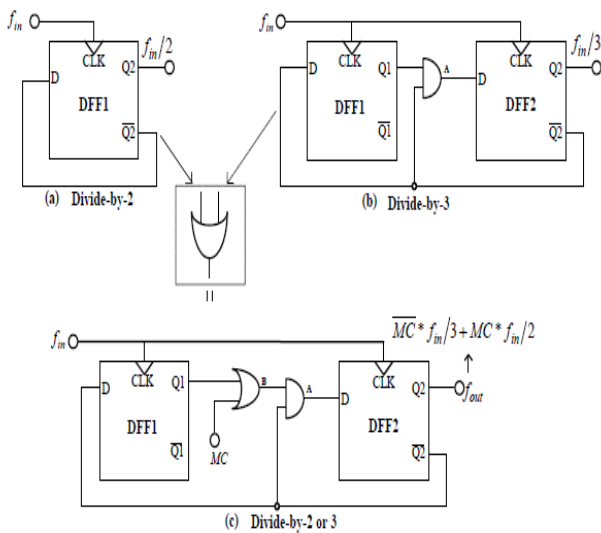


Fig 3 . Synchronous 2/3 Prescaler a) Divide-by-2 circuit b) Divide-by-3 circuit c) Divide-by-2/3 circuit

Frequency dividers are designed based on digital counters that cannot be realized by standard digital circuits. These digital counters cannot be synthesized directly using Register Transfer Level (RTL) description which depend on standard cells as high frequency of operation involves precise design and optimization.

C. Conventional Synchronous TSPC 2/3 Prescaler

The conventional TSPC 2/3 prescaler consists of an AND gate, an OR gate and two D Flip-Flops (DFF). Due to the large load on DFF2 the speed of conventional 2/3 prescaler may go down and further decreases with the difficulty to implant the OR and AND gates into the DFF. This also causes substantial power dissipation in addition to delay [2,3].

The total load capacitance at the output node Q_b of the conventional 2/3 prescaler is also calculated.

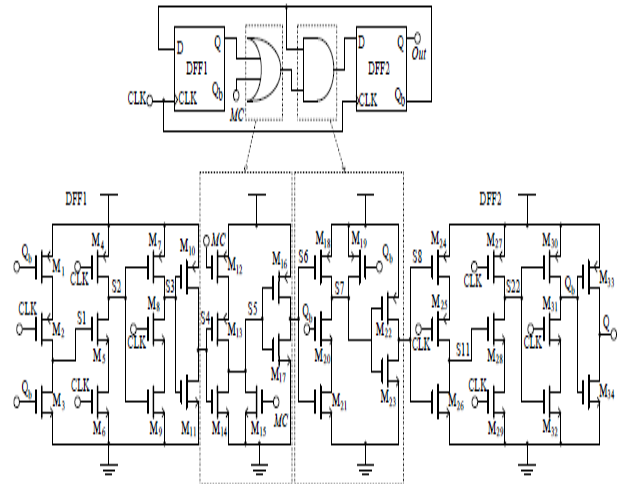


Fig 4. Conventional TSPC 2/3 prescaler and its equivalent gate level schematic.

D. Analysis of tspc 32/33 (n/n+1) prescaler

To verify the advantages of the proposed ultra-low power prescaler, a divide 32/33 dual modulus unit is implemented with the 2/3 prescaler as shown in Fig 5. In this 32/33 prescaler, the proposed 2/3 prescaler unit is followed by four stages of the toggled TSPC divide-by-2 units [6, 7]. Figure 6 shows the complete block diagram of frequency synthesizer using PLL.

$$f_{32} = (AD - MOD) * X(M) + (MOD * X(M + 1)) \dots\dots (2)$$

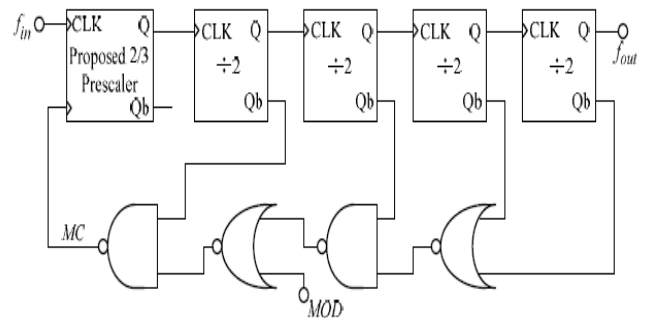


Fig 5 . TSPC 32/33 prescaler using 2/3 prescaler.

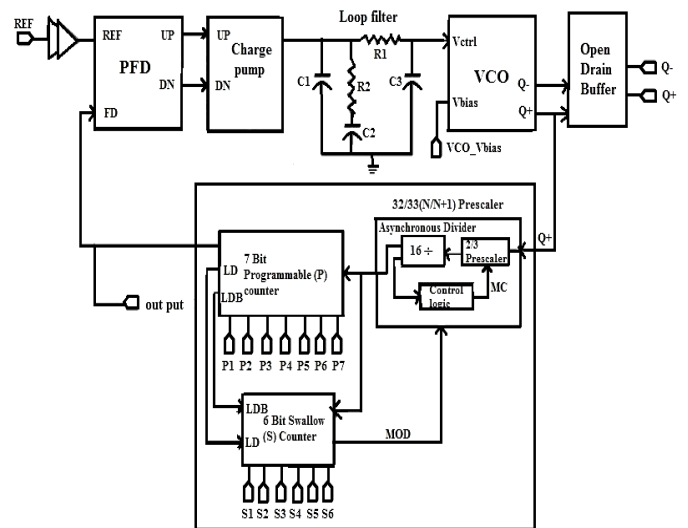


Fig 6. PLL frequency synthesizer

E. Fully Programmable Divider

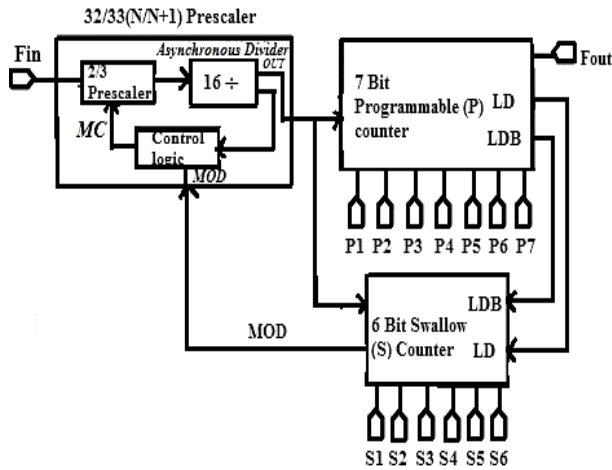


Fig 7. Fully Programmable Divider

For PLL synthesizers operating in the 2.4 GHz and 5.4 GHz ISM band with a resolution of 2.4 MHz and 3.5 MHz division ratios of 2400-5400 can be achieved with a 32/33 prescaler, a 7 bit P-counter and a 5 bit S-counter. Fig 7 shows the Design of fully programmable divider with a division ratio from 2400 to 2484 in steps of 1. In this design, only bits P1, P2 and P3 of the P-counter are used. Programming of the bits P4, P5, P6 and P7 are fixed at ‘1’, ‘0’, ‘0’, and ‘1’ respectively to have P-values from 74-77[4,5,8]. Here all the bits of S-counter are used for programming. The P and S counter’s programmable value for the division ratios from 2400 - 2484 is shown in Table 1.

Table 1. Programmable Values Of The Programmable Counters

Frequency division ratio	Prescaler (N/N+1)	Programmable Counter (P)	Swallow counter (S)
2400-2431	N=32	P=75	S=0-31
2432-2463	N=32	P=76	S=0-31
2464-2484	N=32	P=77	S=0-20

F. Design of Charge Pump

Charge pump consists of two switched current sources driving a capacitor as shown in figure8. Switching is realized by means of a three-state PD. When the output clock (out_clk) of the delay line lags after the input reference clock (ref_clk), the up signal is high and dn signal is low. The up signal turns on the upper switch and charges the output node Vctrl. On the other hand, when the output clock (out_clk) of the delay line leads before the input reference clock (ref_clk), the up signal is low and dn signal is high. The schematic of an LC VCO used in the design is as shown in figure 9.

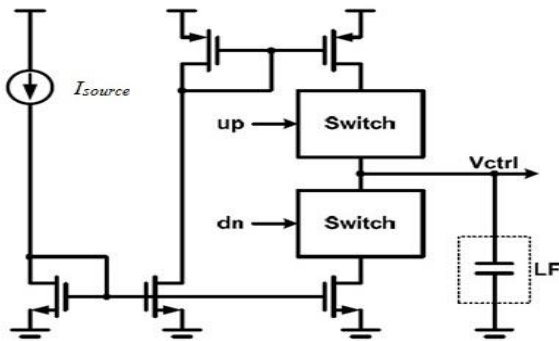


Fig 8. Switched mode Charge Pump

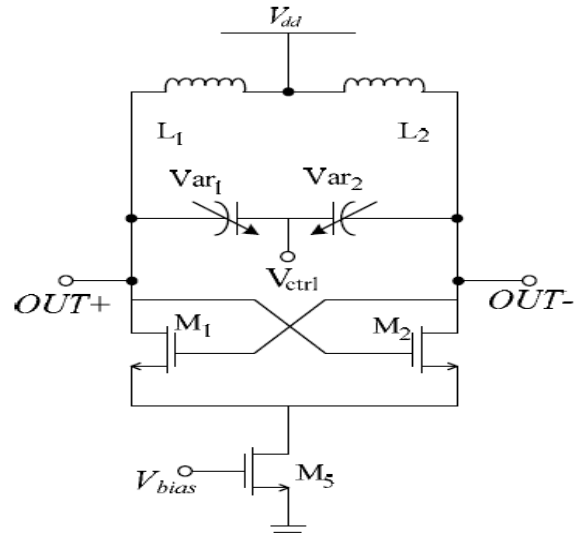


Fig 9. Schematic of an LC VCO.

IV. Results

This work focuses on the design techniques of low power frequency dividers and PLL frequency synthesizers. Using the theory and circuits developed, a 2.4 GHz and 5.4 GHz fully integrated and fully programmable frequency synthesizer individually designed in 180nm CMOS technology using Cadence virtuoso tool. Major building blocks such as TSPC 2/3 prescaler 32/33 prescaler, fully programmable divider and VCO are designed, simulated and verified. The simulation results of TSPC 32/33 prescaler in divide-by-32 mode, Simulation Results of Charge Pump, Simulation of conventional TSPC 2/3 prescaler, simulation result of TSPC 32/33 prescaler in divide by 33 mode, simulation result of 1.8-V, 2.4 GHz PLL frequency synthesizer (Design-I) and simulation results of 1.8-V, 5.4 GHz PLL frequency synthesizer (Design-II) are shown in figure 10 to figure 15 respectively. Frequency synthesizer design specification and power consumption as shown in Table 2.

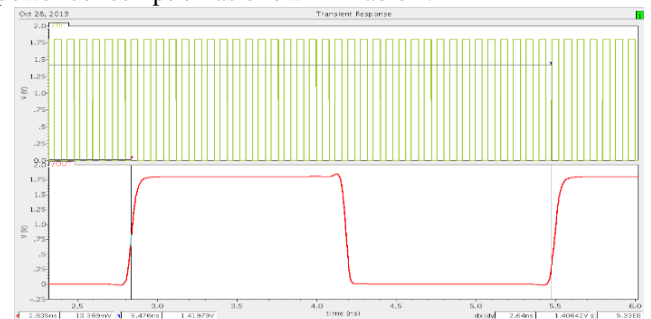


Fig 10.Results of TSPC 32/33 prescaler in divide-by32 mode.

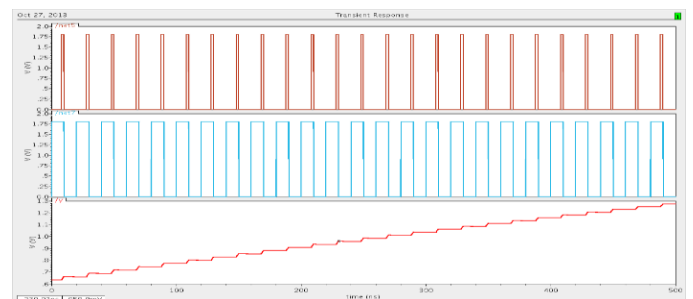


Fig 11. Simulation Results of Charge Pump.

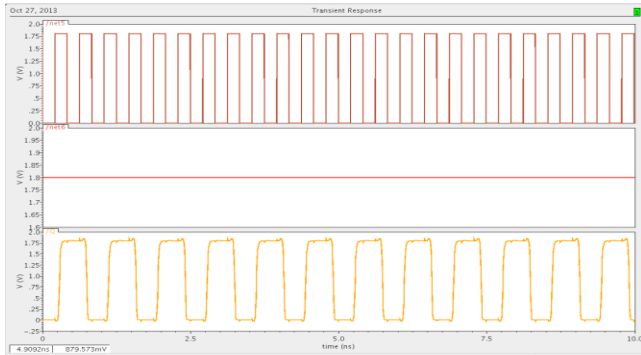


Fig 12. Simulation result of conventional TSPC 2/3 prescaler.

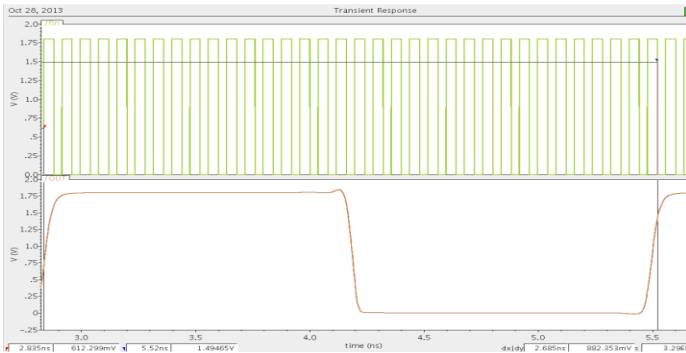


Fig 13. Simulation result of TSPC 32/33 prescaler in divide by 33 mode.

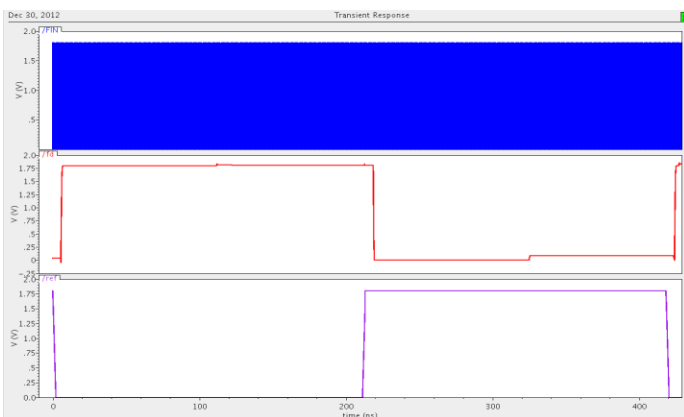


Fig 14. Output of 1.8-V 2.4 GHz PLL frequency synthesizer (Design-I).

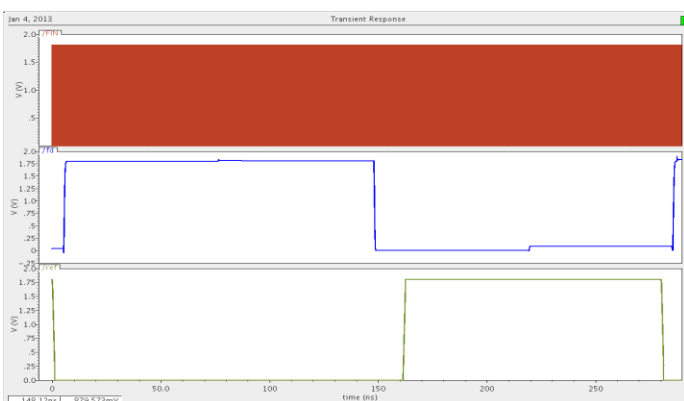


Fig 15. Output of 1.8-V 5.4 GHz PLL frequency synthesizer (Design-II).

Table2. Frequency synthesizer design specifications and power consumption

Design Parameters	32/33 Mode-I	32/33 Mode-II
Process(μm)	0.18	0.18
Power Supply	1.8V	1.8V
Frequency	2.4GHz	5.4GHz
Resolution	2.3MHz	3.5 MHz
Power Consumption	7.719 mW	9.874 mW

5. Conclusion

The different kinds of divider topologies are verified. Propagation speed and power consumption of dynamic logic dividers such as TSPC and E-TSPC circuits are calculated. Based on this, a new low power and improved speed TSPC 2/3 prescaler is proposed and verified in the design of a 32/33 prescaler. Compared with the existing TSPC architectures, the proposed 2/3 prescaler is capable of operating up to 5.4 GHz. In the proposed 2/3 prescaler, wide band 2/3 prescaler, 32/33 prescaler and the fully programmable divider, only the switching, short-circuit power and propagation speed are analyzed. Noise analysis has not been performed on these dividers as fully programmable divider noise contributes to the close-in phase noise of the PLL. The proposed dynamic dividers maximum operating frequency is limited below 5.5 GHz and the future work can be focus on improving the maximum operating frequency at lower power levels in alternative technologies.

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