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Design and FPGA Control of Modular Multilevel Inverter for Photovoltaic Applications

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ABSTRACT

Recently, modular multilevel inverter(MMLI) have gained interest for photovoltaic applications. This topology minimizes the total harmonic distortion both at the DC and AC side and reduces the voltage stress across the devices for high voltage applications compared to the conventional multilevel inverter. This paper explains the significance of a MMLI by employing phase shift PWM technique. This control algorithm is implemented in SPARTAN/FPGA board. The important aspect of this paper is the issues related to capacitor voltage balancing is addressed. The MMLI is powered by PV source and the modeling of PV alongwith MPPT is implemented in MATLAB. The validity of the proposed modular MLI topology is confirmed by simulation and experimentation.

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1. Introduction

Photovoltaic system is the well accepted renewable source and it is suited for power generation from low to high power applications. PV systems can be used for standalone or grid connected system. For grid connected systems, two -level and multilevel inverters are employed. But the two-level inverter suffers from high harmonic distortion, high voltage stress across the devices and high switching losses. To overcome this, multilevel inverters were employed for PV grid connected system [1]. MLI suffers from high voltage stress, therefore, a modular MLI is proposed in this paper. The proposed MMLI is an alternative solution to the conventional two-level inverter as it minimizes the harmonic distortion, voltage stress for high voltage application and possess fault ride through capability[2-3]. A nine-level MMLI is discussed in this paper. Various modulation methods have been discussed in the literature[4-5]. But this paper focuses on the phase shift carrier based PWM technique as it provides a reduced total harmonic distortion and balanced switching actions. The PWM technique is implemented using SPARTAN/3E for better accuracy. Moreover, the problem of capacitor voltage balancing is also investigated in this paper by developing a suitable algorithm. Simulation studies of the proposed inverter is studied in MATLAB/SIMULINK and PWM is generated in Xilinx/Spartan. The theoretical results are verified practically.

2. Modular Multilevel Inverter

The modular multilevel inverter(MMLI) topology is based on the cascaded interconnection of half-bridge switching sub-modules(SMs or cells) [6].It consists of half-bridge cells cascaded in series which forms the phase-legs of the converter. Each leg consists of an upper and a lower arm consisting of series of SMs and an arm inductor.

The inductor serves the purpose of limiting the short circuit current through the leg. As the cells are connected in series, the current through the arm flows through each of the cells and affects the voltage of the capacitor. The capacitor charges and discharges as the positive and negative current flows through it. To understand the operation of the proposed MMLI, let us consider a single cell of modular multilevel converter as shown in Fig.1.Here, when main switch, S_m is on and when auxiliary switch, S_c is off, the output voltage is zero. When S_m is off and S_c is on, the output voltage is $V_o = V_{dc}$. Table .1 shows the switching states of a cell.

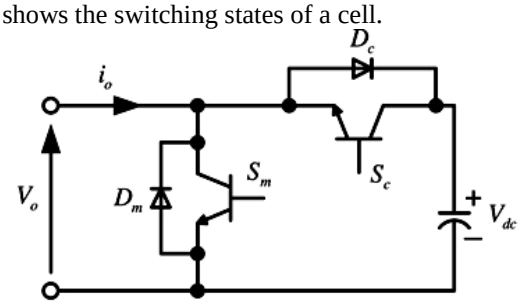

Fig 1. Structure of single cell of MMLI.

For a nine level modular multilevel inverter as shown in Fig.2, there are (2n-2) capacitors and (n-1) cells in both upper and lower arm i.e. there are four capacitors and four cells in each arm. In the nine level MMLI, there are 70 switch states for each phase. These can be used collectively to generate a nine-level output in each phase of the inverter. The capacitance and inductance selection is based on the circulating current and voltage ripple across sub-module capacitors. The selection of capacitance and inductance of MMLI is very essential as proper selection of such parameters drastically reduces the circulating current ac component, converter power losses and sub-module capacitor voltage ripples.

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Table 1. Switching states of a single cell.

S_M	S_C	V_0	CURRENT DIRECTION	POWER PATH	CAPACITOR STATE
On	Off	0	$i_0 > 0$	S_m	Unchanged
On	Off	0	$i_0 < 0$	D_m	Unchanged
Off	On	V_{dc}	$i_0 > 0$	D_c	Charging
Off	On	V_{dc}	$i_0 < 0$	S_c	Discharging

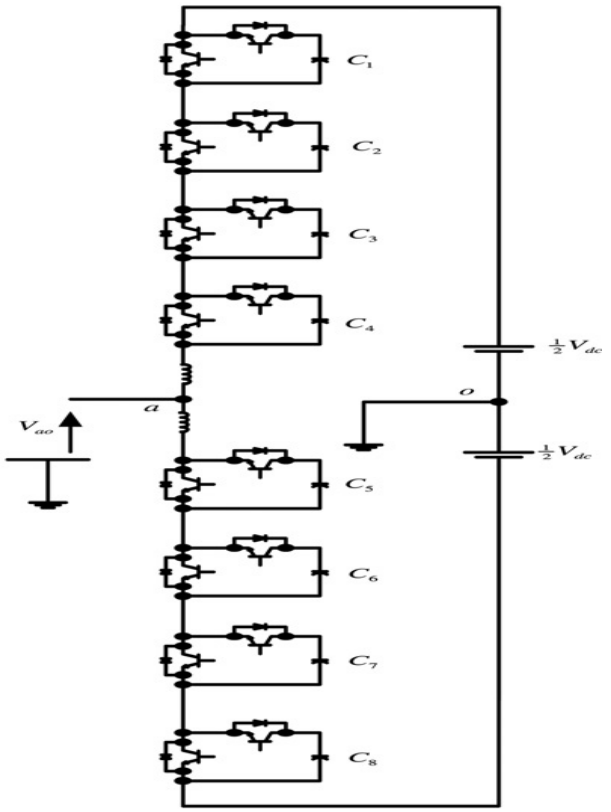

Fig 2. Power circuit of nine- level modular multilevel inverter.

3. Phase Shifted Pwm (PS-PWM)

The phase shifted and level shifted are the two most commonly employed sub-harmonic PWM schemes for multilevel inverters. Phase-shifted multicarrier modulation is derived from unipolar modulation and it is discussed in this paper. The expression indicating the relation between the numbers of carriers and the number of voltage levels is shown in Eq. 1. All carriers must have the same frequency and peak-to-peak amplitude. Eq. 2 gives the phase difference between two carriers.

Number of carriers = (number of voltage levels -1) (1)

Phase shift of the carriers = (360/ (number of voltage levels -1)) (2)

Fig.3 shows the carrier waveforms and sinusoidal reference of phase shifted PWM.

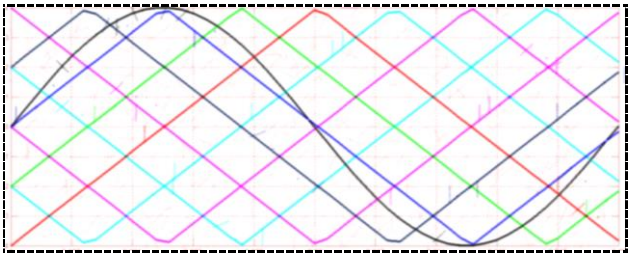

Fig 3. Comparison of triangular carriers with the sinusoidal reference.

The best suited strategy for the modular multilevel inverters[7] is PS-PWM because of the two important reasons:

1.PS-PWM has the inherent voltage balancing because of which the capacitor voltage balancing is not mandatory for the MMLI with PS-PWM as the modulation strategy.

2.The current THD for the PS-PWM technique is the least when compared with the other PWM techniques.

4. FPGA Implementation

The gating pulses to the switches is given by the FPGA Xilinx Spartan 3A DSP kit. The coding is obtained from the Xilinx software integrated with the matlab. The stages in the development of the code using Xilinx software consists of generation of reference sine wave and triangular carrier wave. The reference sine wave generation is shown in Fig.4. The Xilinx counter block implements a free running or count-limited type of an up, down, or up/down counter. The counter output can be specified as a signed or unsigned fixed-point number. Free running counters are the least expensive in FPGA hardware. The output of the counter is ramp signal which is given to the ROM block. The Xilinx ROM block is a single port read-only memory (ROM). Values are stored by word and all words have the same arithmetic type, width, and binary point position. Each word is associated with exactly one address. An address can be any unsigned fixed-point integer from 0 to d-1, where d denotes the ROM depth (number of words). The memory contents are specified through a block parameter. The block has one input port for the memory address and one output port for data out. The address port must be an unsigned fixed- point integer. The output of ROM is the sine wave. The delay is used in order to have the sinusoidal reference to start from zero. The sinusoidal reference obtained by using Xilinx block set is shown in fig.5 .

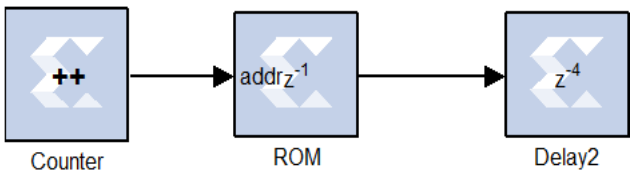

Fig 4. Generation of reference sine wave using Xilinx blockset.

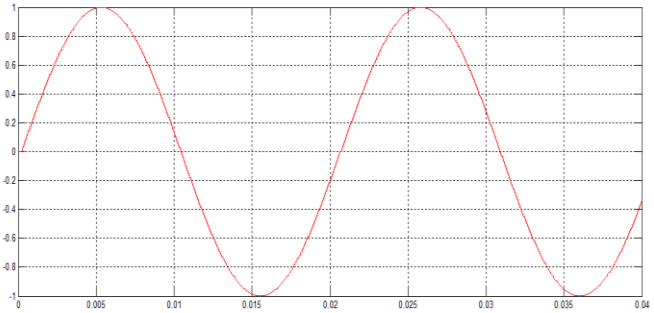

Fig 5. Sine wave output using Xilinx blockset

4.1. Generation of Triangular Carrier

The generation of triangular carrier using Xilinx block set is shown in Fig.6.The counter is used to generate the ramp signal. The output of the counter is sliced and inverted. The Xilinx slice block allows to slice off a sequence of bits from the input data and create a new data value. This value is presented as the output from the block. The output data type is unsigned with its binary point at zero. The block provides several mechanisms by which the sequence of bits can be specified. If the input type is known at the time of parameterization, the various mechanisms do not offer any gain in functionality. If, however, a slice block is used in a design where the input data width or binary point position are subject to change, the variety of mechanisms becomes useful. The block can be configured, for example, always to extract only the top bit of the input, or only the integral bits, or only the first three fractional bits. The counter output is nothing but the sliced pulses based on which the up/down counter counts. The output of up/down counter is triangular wave but its magnitude is not unity. In order to have the magnitude unity constant and multiplier blocks are used. Thus by using the blocks shown in fig.6 triangular carrier of magnitude unity is generated. Fig.7 shows the triangular carrier output using Xilinx block set.

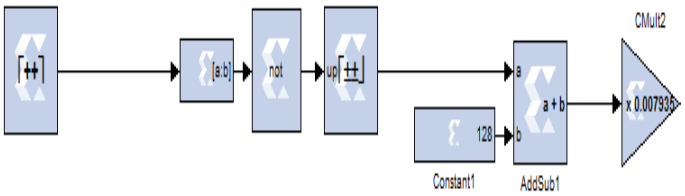

Fig 6. Generation of triangular carrier using Xilinx blockset..

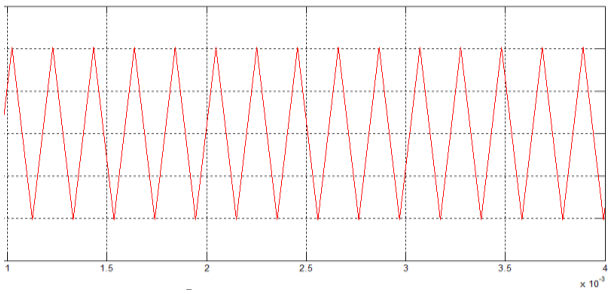

Figure 7. Triangular carrier output using Xilinx blockset

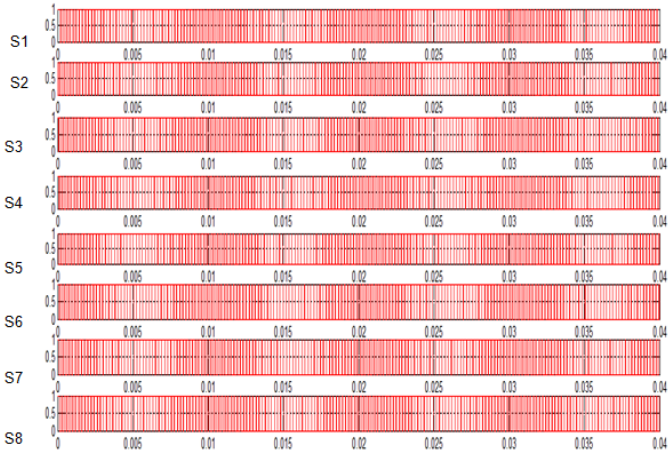

Figure 8. Gating pattern for the eight main switches using xilinx block set.

By comparing the sine wave with that of the triangular carrier the pulses are obtained. Fig.8 shows the pulses to be given to the eight main switches of the modules of MMLI. The simulation parameters of the nine level modular multilevel inverter is shown in table.2. Based on the simulation parameters the output voltage and current waveforms are obtained as shown in Fig.9.

Table 2. Simulation parameters of nine level MMLI.

Modulation index, m_a	1
Frequency of modulation, m_f	99
Arm Inductance (L_{arm}) and arm resistance (R_{arm})	30 mH, 0.1Ω
Load resistance, R_L	150Ω
Load inductance, L_L	150mH.
Sub-module capacitance,C_{sm}	3.33mF
Voltage reference, V_{ref}	24 volts
Frequency, f	50 Hz

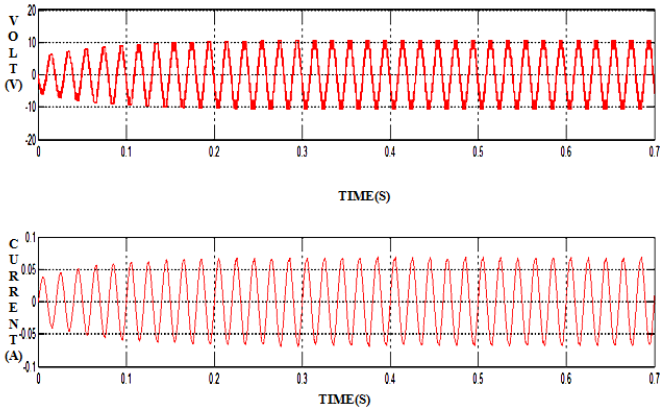

Figure 9. Output voltage and output current waveforms of nine level MMLI.

The performance parameters such as total harmonic distortion (THD), First-order distortion factor (DF_1), Second-order Distortion factor (DF_2) and switching losses have been evaluated using matlab. It was found that the proposed strategy has reduced THD.

Table 3. Performance parameters of PS-PWM.

PERFORMANCE PARAMETERS	PS-PWM
THD	13.86%
DF_1	26%
DF_2	11.2%
WTHD	6.2%
HSF	79.26%

Table 3 shows the performance parameters of phase shifted PWM technique. The values of the obtained performance parameters shows that PS-PWM is suitable method and most feasible for the modular multilevel inverter.

5. Capacitor Voltage Balancing Of Modular Mli

Even though phased shifted technique provides the best performance in terms of balancing, the problem persists. A constant predefined pattern will connect the same sub modules at the same current status, causing the same capacitor voltage deviation in every fundamental cycle. Unless treated, the capacitor voltages will diverge causing unbalanced operation and introducing significantly disturbances in the output waveform. A proper control method has to be designed in order to keep the sum of all capacitor voltages stable (averaging) and to ensure the correct voltage share among all individual capacitors (balancing), without any external balancing circuit[8]. The averaging control relies on adjusting the circulating current from the DC link to the phase leg.

While the balancing control, which is characterized by reducing the average voltage difference between the positive and negative arms. Using the two control loops enables the converter to realize the stable voltage control in all operating conditions. Thus the voltage-balancing control of eight floating dc capacitors per leg can be mainly divided into:

1) Averaging control
2) Balancing control.

In averaging control, It forces the *u*-phase average voltage V_{acu} to follow its command Vc as shown in Fig.10.

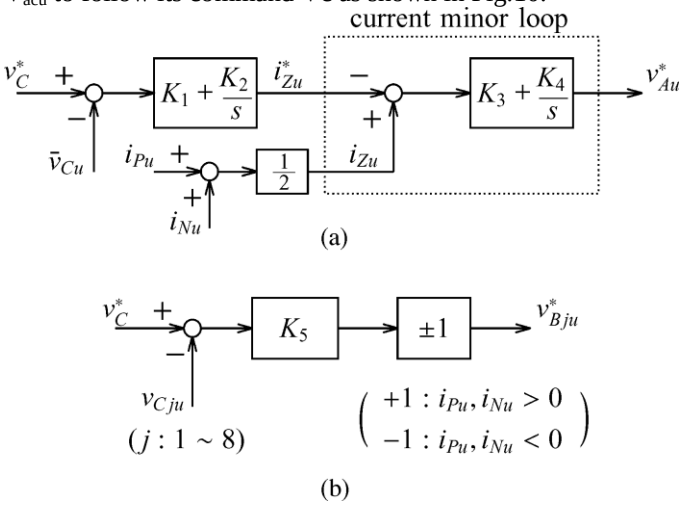

Figure 10. Block diagram of dc-capacitor voltage control: (a) Averaging control,and (b) Balancing control.

The use of the balancing control forces the individual dc voltage to follow its command V_c^* .Figure 10(b) shows a block diagram of the single phase balancing control, where V^*_{Bju} is the voltage command obtained from the balancing control. The control gains used for capacitor voltage balancing is shown in the table 4.

Table 4. Control gains used for capacitor voltage balancing.

PARAMETERS	CONSTANT	VALUE
Proportional gain of averaging control	K1	0.5 A/V
Integral gain of averaging control	K2	150 A/(V.s)
Proportional gain of current control	K3	1.5 V/A
Integral gain of current control	K4	150 V/(A.s)
Proportional gain of balancing control	K5	0.35

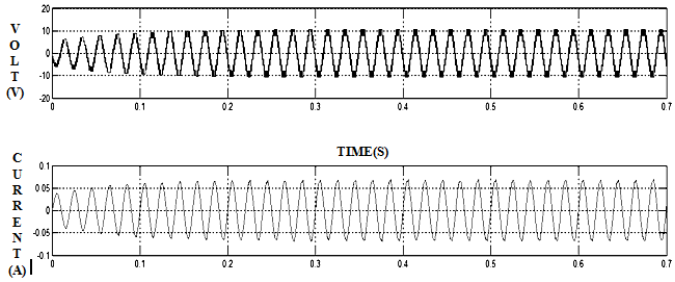

Figure 11. Output voltage and current waveforms of nine level MMLI using capacitor voltage balancing.

The simulation output of voltage and current of nine level modular multilevel inverter using capacitor voltage balancing is shown in figure 11. The capacitor voltage balancing is done basically to improve the output voltage and output current waveforms. By implementing the capacitor voltage balancing the efficiency of the outputs is improved. Thus capacitor voltage balancing becomes mandatory in order to have a highly efficient modular multilevel inverter.

6. Application of Mmli for Photovoltaic Applications

Fig.12 shows the Matlab/Simulink model of PV model of open circuit voltage 12 volts and fig.13 shows the characteristics of PV model.

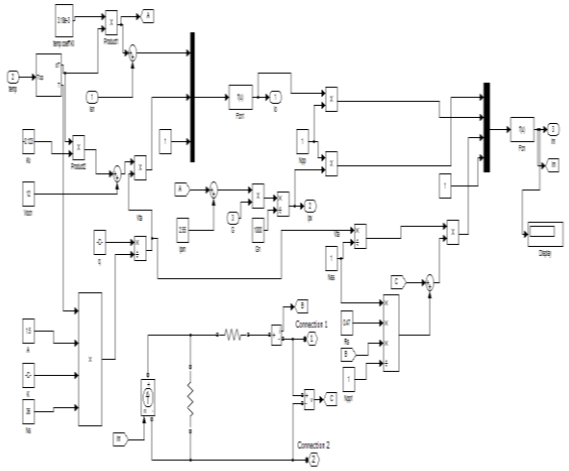

Figure 12. PV model of open circuit voltage 12 volts

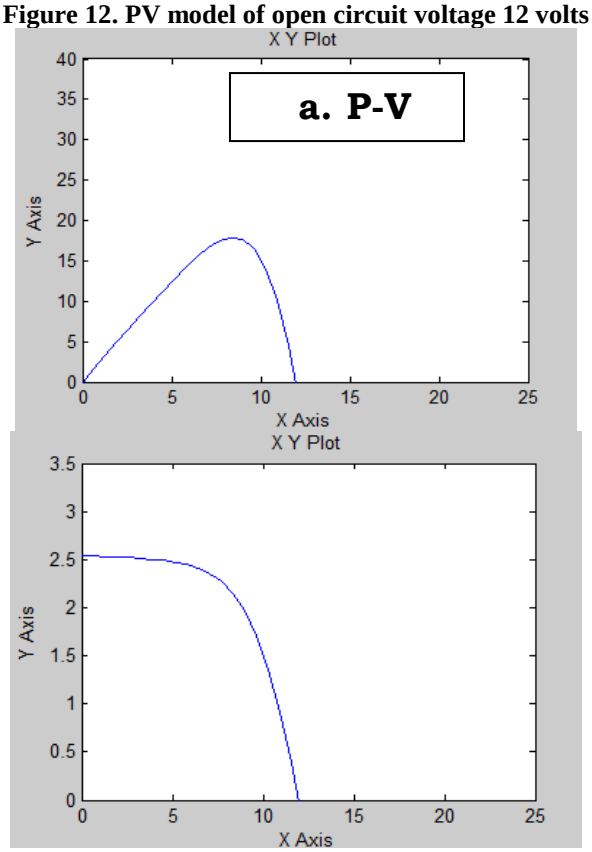

Figure 13. a P-V characteristics of PV model b. I-V characteristics of PV model.

The idea here is to obtain the maximum power from the PV panel using incremental conductance method of maximum power point tracking technique and the obtained pulses is given to the boost converter whose output is used as the dc source for the modular multilevel inverter[9]. Fig.14 shows the Matlab/Simulink model of incremental conductance method of MPPT. Fig.15 shows the output pulses that is obtained from the pulse generator which is being driven by the duty cycle of 0.5 and duty cycle correction from the incremental conductance method as shown in Fig.14.

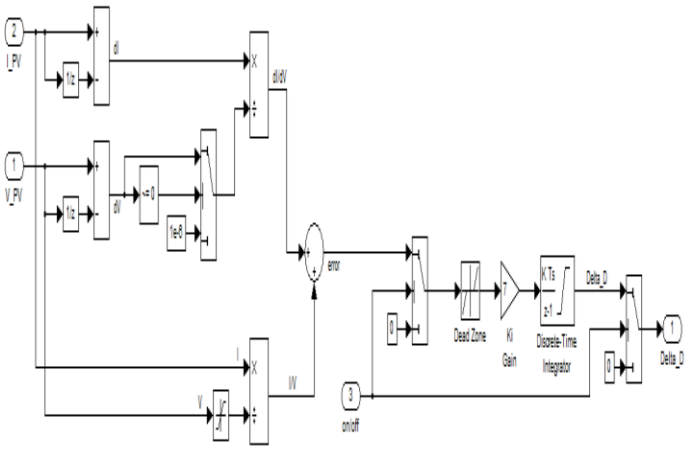

Figure 14. Incremental conductance method.

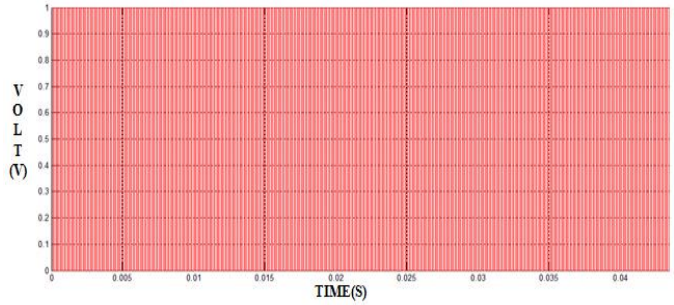

Figure 15. Output pulses from pulse generator

By using the pulse as shown in figure 6.4 to trigger the boost converter and using the output of the boost converter as dc source to the modular multilevel inverter the solar energy could be effectively utilized. Thus modular multilevel inverter is one of the promising topology that could be used for renewable energy applications especially solar energy.

7. Pcb Design of a Module of Mmli

The single module of the M2LI is designed by using eagle software. The designed module is then etched on a copper cladded sheet. Then the components are soldered on the copper cladded sheet. Fig.16 shows the PCB design of the single module of MMLI using eagle software.Fig.17 shows the single module of five level MMLI. The single module consists of two IRF840 Mosfets, two 4N35 optocouplers, two 100 µF and one 1000 µF capacitors, two w10 bridge rectifiers, two LM7812 voltage regulators and two 330Ω resistors, two 10KΩ resistors and two 10Ω resistors[10].

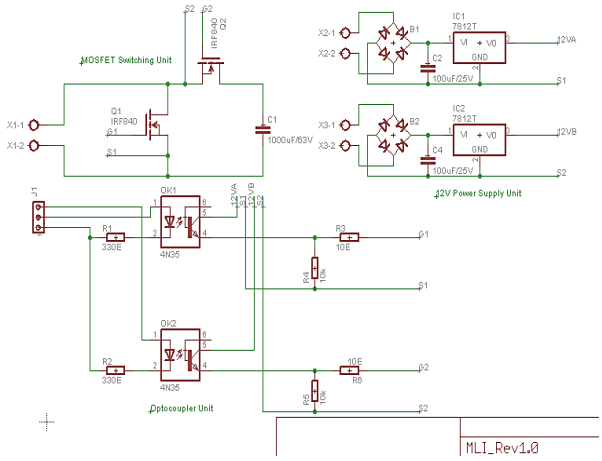

Figure 16. PCB design of a single module of five level MMLI

The output from the 230/(15-0-15) volt transformer is rectified by means of bridge rectifier and the rectified output voltage is given to the voltage regulator which regulates the output voltage to 12 volts. These forms the power supply to a single optocoupler. Similarly for the next optocoupler power supply is made. The output from the FPGA PWM pins is given to the optocoupler pins 1 and 2. Pin 3 and 6 of optocoupler is unconnected and the pin 5 is given with 12 volts. The output is measured from the resistor that is connected across 4th pin of optocoupler and ground. This output is given to the gate and source of the mosfet. Thus a single module is completed.

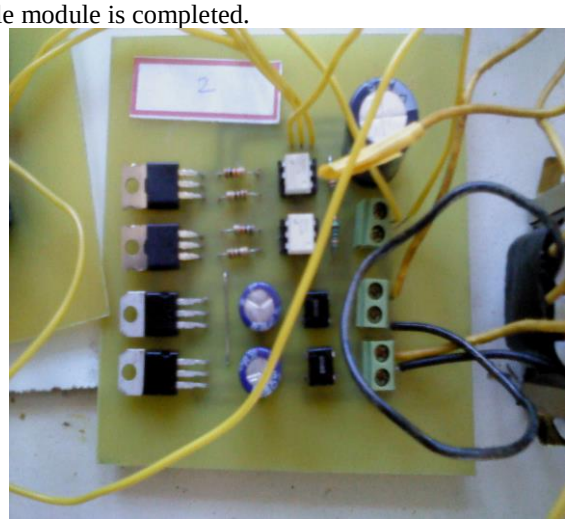

Figure 17. Single module of five level M2LI

Fig.18 shows the entire hardware setup of the five level M2LI. Eight single modules are connected in order to obtain nine level voltage output. The upper arm consists of four modules and the lower arm has four modules. The fourth module of upper arm and the first module of the lower arm is connected with the resistor of 25Ω and inductor of 30mH each in order to limit the inrush current during transients and faults. The nine level output voltage is measured across RL load (150Ω and150mH).

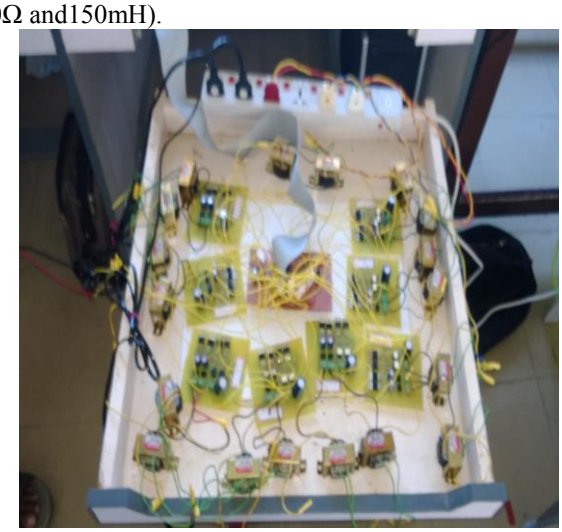

Figure 18. Hardware setup of five level M2LI.

The hardware implementation of the five level MMLI consists of creating FPGA coding to provide gating pulses to the switches, design of the power circuit. The Xilinx Spartan 3A DSP kit is utilized to provide gating pulses and the power circuit is designed using eagle software and etched. The five-level output is shown in Fig.19

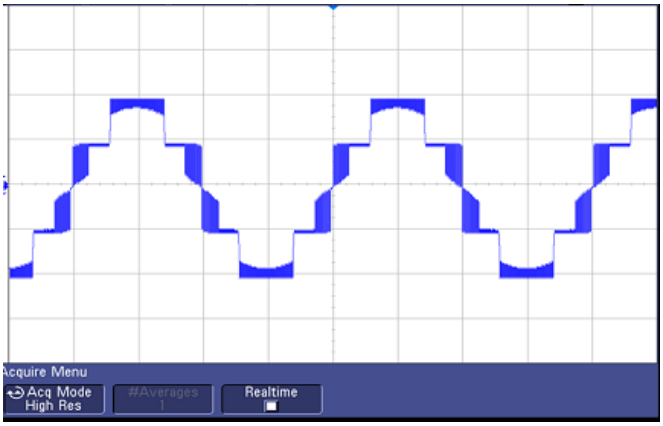

Fig 19. Five-level output voltage of MMLI

8. Conclusion

This paper has investigated the suitability of modular multilevel inverter for photovoltaic applications. PSPWM is implemented using FPGA control as it provided reduced harmonics and balanced switching actions. Moreover, the capacitor voltage balancing techniques for the proposed MMLI is discussed in this paper. From the computed performance parameters, it is found that the PSPWM technique for MMLI results in improved spectral quality of the output. MMLI is interfaced with PV module by employing MPPT and therefore MMLI is a preferred topology for PV applications.

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