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Awakening to Reality

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Implementation of Binary Addition using Brent-Kung Adder

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ABSTRACT

Adders are the most vital part of any digital system. Providing an efficient adder design which satisfies the tradeoff between speed and space aides in increasing the performance of the system. parallel prefix adders are the ones widely used in digital design. This is primarily because of the flexibility in designing the adders. Brent Kung adder is low power adder, as it uses minimum circuitry and also decreases the speed and memory to obtain the result. The 16-bit design is extended to 32-bit, implemented in the physical level.

1. INTRODUCTION

Addition operation is the main operation in digital signal processing and control systems. The fast and accuracy of a processor or system depends on the adder performance. In general purpose processors and DSP processors the addition operation addresses are taken from simple Ripple Carry Adder. It is used for the addition operation i.e., if N-Bits addition operation is performed by the N-Bit Full Adder. In Ripple Carry Adder each Bit Full Adder operation consists of sum and carry that carry will be given to next Bit Full Adder operation, that process is continuous till the Nth bit operation. The N-1thBit Full Adder operation carry will be given to the Nth Bit Full Adder operation present in the Ripple Carry Adder.

Adders are commonly found in the critical path of many building blocks of microprocessors and digital signal processing chips. Its purpose is to form the arithmetic sum of two binary numbers. The most important for measuring the quality of adder designs in the past were propagation delay, and area. Instead of waiting for the carry propagation of the first addition, the idea here is to overlap the carry propagation of the first addition with the computation in the second addition, and so forth, since repetitive additions will be performed by a multi operand adder. In multiplication and division, multi operand addition is often encountered. More powerful adders are required which can add many numbers instead of two together. The design of a high-speed multi operand adder called Parallel Prefix Adders.

In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic units, but also in other parts of the processor, where they are used to calculate addresses. When three or more operands are to be added simultaneously, using two operand adders, the time consuming carry-propagation must be repeated several times. If the number of operands is k, then carry has to propagate (k-1) times. Several techniques for multiple operand addition that attempt to lower the carry propagation have been proposed and implemented. This operator is associative hence it can be implemented in a parallel fashion called Parallel Prefix Adders.

The Prefix outcome of the operation depends on the initial inputs. The Parallel involves the execution of an operation in parallel. This is done by segmentation into smaller pieces that are computed in parallel. This operator is associative hence it can be implemented in a parallel fashion. Different topologies for the parallel generation of carries. Adders that use these topologies are called Parallel Prefix Adders.

Parallel algorithms for prefix sums can often be generalized to other scan operations on associative binary operations and they can also be computed efficiently on modern parallel hardware. Many parallel implementations follow a two pass procedure where partial prefix sums are calculated in the first pass on the each processing unit; the prefix sum of these partial sums is then calculated and broadcast back to the processing units for a second pass using the now known prefix as the initial value. Asymptotically this method takes approximately two read operations and one write operation per item.

An early application of parallel prefix sum algorithms was in the design of binary adders, Boolean circuits that can add two n-Bit binary numbers. In this application, the sequence of carry bits of the addition can be represented as a scan operation on the sequence of pairs of input bits, using the majority function to combine the previous carry with these two bits.

Each bit of the output number can then be found as the exclusive or of two input bits with the corresponding carry bit.

Parallel-prefix adders will have a different performance than VLSI implementations. In particular, most modern FPGAs employ a fast-carry chain which optimizes the carry path for the simple Ripple Carry Adder.

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The Ladner-Fischer is the Parallel Prefix Adders used to done the addition operation. It is look like tree structure to perform the high speed arithmetic operation. Ladner Fischer Adder is used for high performance addition operation.

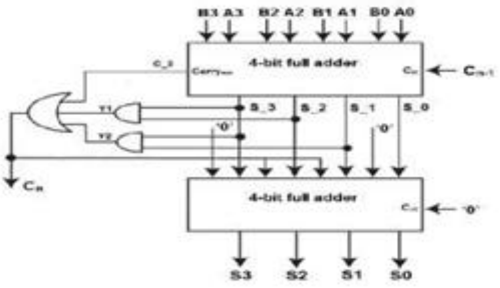


Fig 1.BCD ADDER.

2. BRENT-KUNG ADDER

Brent-Kung adder is a very well-known logarithmic adder architecture that gives an optimal number of stages from input to all outputs but with asymmetric loading on all intermediate stages. It is one of the parallel prefix adders. Parallel prefix adders are unique class of adders that are based on the use of generate and propagate signals. The cost and wiring complexity is less in Brent Kung adders. But the gate level depth of Brent-Kung adders [8] is 0 (log 2(n)), so the speed is lower. The block diagram of 4-bit Brent Kung adder is shown in Fig. 2.

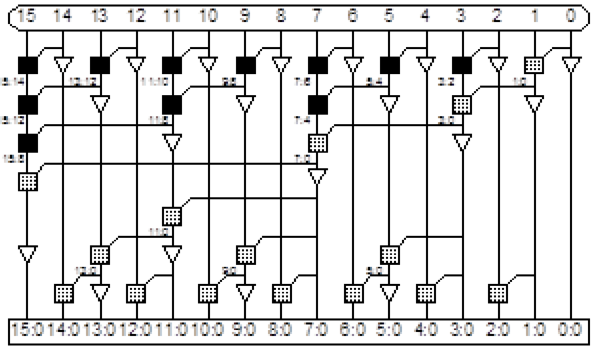


Fig 2. Block diagram of 4-bit Brent Kung adder.

3. PROPOSED SYSTEM

Parallel prefix adders are used to speed up the binary additions as they are very flexible. The structure of Carry Look Ahead Adder (CLA) is used to obtain parallel prefix adders. Tree structures are used to increase the speed of arithmetic operation. Parallel prefix adders are used for high performance arithmetic circuits in industries as they increase the speed of operation.

The construction of parallel prefix adder involves three stages:

1. Pre- processing stage
2. Carry generation network
3. Post processing stage

1. Pre-possessing stage: Generate and propagate signals to each pair of inputs

A and B are computed in this stage. These signals are given by the following equations:

Pi=Ai xor Bi (1)

Gi=Ai and Bi (2)

2. Carry generation network: In this stage, we compute carries equivalent to each bit. Implementation of these operations is carried out in parallel. After the computation of carries in parallel they are segmented into smaller pieces.

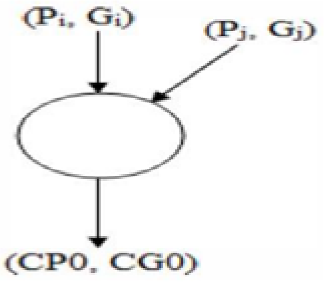


Fig 3. Carry Network.

This is the concluding step to compute the summation of input bits. It is common for all the adders and the sum bits are computed by logic equations.

Ci-1= (Pi and Cin) or Gi

Si=Pi xor Ci-1

3.1 BLACK CELL OPERATION:

Parallel-prefix adders will have a different performance than VLSI implementations. In particular, most modern FPGAs employ a fast-carry chain which optimizes the carry path for the simple Ripple Carry Adder.

The propagate gives "XOR" operation of input bits and generates gives "AND" operation of input bits. The propagate (P_i) and generate (G_i) are shown in below equations 3.1&3.2.

$P_i = A_i$ XOR B_i-------------- (3.1)

$G_i = A_i$ AND B_i-------------- (3.2)

Parallel-prefix adder consists of black cells and gray cells. Each black cell consists of two AND Gate operations and one OR Gate operation shown in fig 4.

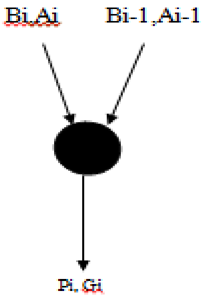


Fig 4. Black cell.

In black cell, CP_i denotes propagate and it consists of only one AND Gate given in equation 3.3. CG_i denotes generate and it consists of one AND Gate and OR Gate given in equation 3.4.

$CP_i = B_i$ AND B_{i-1} -------------- (3.3)

$CG_i = A_i$ OR [B_i AND A_{i-1}] ---- (3.4)

3.2. GRAY CELL OPERATION:

Each gray cell consists of one AND Gate operations and one OR Gate operation shown in fig.5.

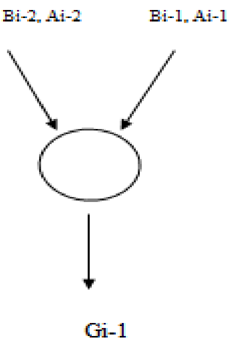
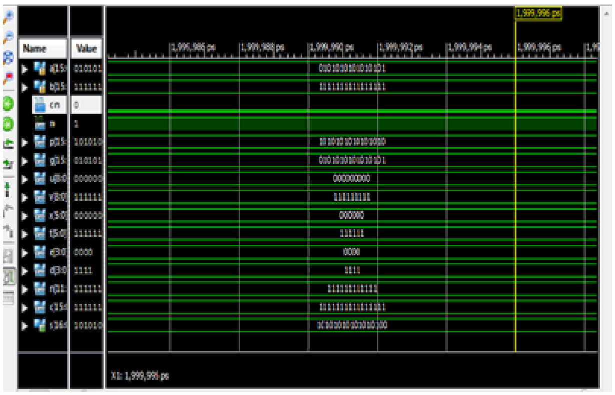


Fig 5. Gray cell

In gray cell, CG_i denotes generate and it consists of one AND Gate and OR Gate given in equation

$CG_{i-1}=A_{i-2}$ OR $[B_{i-2}$ AND $A_{i-1}]$ --- (3.5)

SIMULATION RESULTS



Software Requirements:

- ➢ MODELSIM 6.4b
- ➢ XILINX 10.1

It requires Xilinx ISE 10.1 version of software where verilog source code can be used for design implementation.

4. CONCLUSION

In this project, a new approach to design an Efficient Brent Kung Adder concentrates on gate levels to improve the speed and decreases the memory. It is like tree structure and cells in the Carry Generation Stage are decreased to speed up the binary addition. The Proposed Adder addition operation offers great advantage in reducing delay.

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